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TECHNICAL MEMORANDUM

THREE-PHASE INVERTER FOR SMALL HIGH SPEED MOTORS

TM-1499 JULY 1991

Creare

THREE-PHASE INVERTER FOR SMALL HIGH SPEED MOTORS

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16. Abstract

A high-frequency three-phase inverter is being developed to drive a miniature centrifugal compressor which is a key component in a long-life space-borne cryocooler. The inverter is a unique transformer-coupled design, tailored to the low-voltage high-current characteristic of the compressor's induction motor. This report describes the design and performance demonstration of a breadboard model of the inverter.

The cryocooler uses a reverse-Brayton cycle with turbomachines to provide 5 watt of cooling at 70 K. The design target for input power to the compressor motor is 175 watts. Line-to-neutral phase voltage waveforms to be supplied by the inverter have an amplitude of 15 volt-rms at a frequency of 8 kHz. DC power at 28 volt is supplied to the inverter. The breadboard inverter was tested with a preliminary development model of the compressor. It drove the compressor over a range of operating conditions encompassing frequencies of 5 to 9 kHz at powers of 56 to 437 watt. Inverter efficiencies, calculated from experimentally verified loss models, ranged from 89 to 95% over the tests. The design target on efficiency is 90%. The inverter was demonstrated to supply starting current adequate to overcome the starting friction of the compressor's self-acting gas bearings by a safe margin.

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LIST OF SYMBOLS

A_{core}	Cross-sectional area of toroid
B	Magnetic flux density in toroid
B_{max}	Maximum value of B
c_p	Heat capacity at constant pressure
C_b	Bootstrap capacitance
C_c	Timing circuit capacitance
D_i	Inner diameter of toroid
D_o	Outer diameter of toroid
f	Inverter frequency
f_c	Clock frequency
f_s	Rotational frequency of motor
h	Height of toroid
H_s	Isentropic enthalpy rise for compressor
i_0	DC current supplied to inverter
i_a	Primary current for "a" transformer
i_{a0}	Amplitude of i_a waveform
i_b	Primary current for "b" transformer
i_{b0}	Amplitude of i_b waveform
i_m	Current in one motor phase
i_{m0}	Amplitude of i_m waveform
i_p	Current in primary lead
i_{p0}	Amplitude of i_p waveform
i_r	Component of i_m in load resistance
i_x	Component of i_m in load inductance
K_c	Coefficient in core loss expression

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LIST OF SYMBOLS (continued)

L	Load inductance
m	Frequency exponent in core loss expression
m	Net mass flow rate of compressor
n	B_{max} exponent in core loss expression
N_{pa}	No. of primary turns for "a" transformer
N_{pb}	No. of primary turns for "b" transformer
N_{sa}	No. of secondary turns for "a" transformer
N_{sb}	No. of secondary turns for "b" transformer
p_1	Compressor inlet pressure
p_2	Compressor exit pressure
PR	p_2/p_1
r	Radial coordinate for toroid B field
R	Load resistance for one phase
R_c	Timing circuit resistance
R_{ds}	MOSFET drain-to-source on resistance
R_{pa}	Primary coil resistance for "a" transformer
R_{pb}	Primary coil resistance for "b" transformer
R_{sa}	Secondary coil resistance for "a" transformer
R_{sb}	Secondary coil resistance for "b" transformer
R_x	Resistance of load inductor for one phase
s	Induction motor slip: $(f - f_s)/f$
t	Time
T_1	Compressor inlet temperature
V_{core}	Volume of toroidal core
V_0	DC voltage supplied to inverter

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LIST OF SYMBOLS (concluded)

V_a	Voltage across primary coil of "a" transformer
V_b	Voltage across primary coil of "b" transformer
V_m	Line-to neutral voltage for one phase of motor
V_{m0}	Amplitude of V_m waveform
V_p	Voltage at primary lead
V_s	Line-to-neutral voltage for one phase of inverter secondary
W_0	DC power supplied to inverter: $i_0 V_0$
W_{core}	Total core loss for inverter transformers
W_{inv}	Total inverter loss
W_m	Total power supplied to three motor phases by inverter
z_{rds}	Total loss from R_{ds} for all MOSFET's
W_{res}	Total resistive loss for inverter transformer coils
W_s	Isentropic compression power: $m H_s$
X	Reactance of load inductor for one phase: ωL
γ	Ratio of constant volume to constant pressure heat capacities
η_{inv}	Inverter efficiency: W_m/W_0
η_s	Overall isentropic efficiency: W_s/W_0
ϕ_a	Magnetic flux in "a" transformer
ϕ_{a0}	Amplitude of ϕ_a waveform
ϕ_b	Magnetic flux in "b" transformer
ϕ_{b0}	Amplitude of ϕ_b waveform
θ	Power factor angle (i_m lags V_m by θ)
ω	Angular frequency of inverter: $2\pi f$

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EXECUTIVE SUMMARY

This is the final report for a Phase II SBIR project to develop a high frequency three-phase inverter for miniature induction motors. The overall objective of the project is the development and demonstration of a breadboard inverter that supplies 3-phase AC power at low voltage and high current to drive miniature high speed motors. This inverter is a critical component in long life turbo-Brayton cryocoolers that are under development for the cooling of spaceborne sensors. The reverse Brayton thermodynamic cycle in these coolers relies on a miniature motor driven centrifugal compressor running at speeds on the order of 8000 rev/s. High efficiency of the motor-inverter system are paramount, given that cryocoolers are likely to consume a major share of a satellite's electrical power capacity. Long life and high reliability are of major importance, as well, since cryocoolers will need to function untended over multi-year space missions.

Development of the breadboard inverter has been guided by a preliminary specification for a single-stage reverse-Brayton (SSRB) cryocooler being developed for NASA under a concurrent contract (NAS5-31281). The specification calls for the inverter to supply three-phase AC power to the compressor motor at nominally 8 kHz, 15 volt-rms and 7.8 amp-rms per phase, with 175 watt total output. The inverter would draw power from the spacecraft bus at 28 volt-DC. Performance objectives are high efficiency (90% or greater), and low harmonic content in the output waveforms. The key design objective is that the inverter constitute a simple self-contained and compact electronics package offering the potential for high reliability. All objectives were successfully met or exceeded by the project.

The basic concept that has evolved in Phase II is a transformer-coupled inverter. This consists of a network of transformers and power transistor switches. AC output waveforms are assembled at the transformer secondary coils from square waves created by alternately switching the primary coils between the DC input voltage and ground.

In Phase II, a unique configuration using six small toroidal transformers and 12 MOSFET switches was derived from the rotating field inverter (RFI) concept put forth in Phase I. This approach solved the problem of high magnetizing currents caused by the air gap inherent to the design of the single multi-coil transformer in the RFI. In the present six-transformer concept, two of the transformers generate the output voltage for each phase. The turns ratios for the two transformers are fixed in a proportion that minimizes the harmonic content of the voltage waveform. The resulting voltage waveshape has a stepped sinusoidal pattern in which all harmonics below the eleventh are eliminated.

The transformer coupled inverter concept is well suited to the high frequency requirement since low magnetic flux levels at high frequency allow small toroidal cores to be used. Off-the-shelf ferrite toroids worked exceedingly well in the breadboard. Use of higher performance magnetic materials in the future will allow the transformers to be further reduced in size.

As a result of calorimeter measurement of losses in the breadboard inverter, the loss mechanisms are well understood and highly predictable. Losses are calculated from measured currents and electrical resistances in the transformer coils and MOSFET's, and from magnetic properties of the cores. Sizing an inverter for a particular application is a matter of selecting components whose calculated losses at design voltage and current levels will meet the efficiency goal.

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Transformers and MOSFET's for the breadboard were sized conservatively in order to provide a large margin between design point power levels and rated capacity. Based on direct measurement of MOSFET resistance, calculated efficiency of the breadboard inverter is 96.7% at the 175 watt design point. At 350 watts, the efficiency is 93.4%.

Measured voltage and current waveshapes for the breadboard showed close agreement with waveshapes predicted by transformer design relations. Current waveshape irregularities associated with the stepped character of the voltage waveshape are accurately predicted by the design relations. Consistent stable performance of the breadboard inverter in driving a prototype compressor over a wide range of speeds and loads established a high level of confidence in the overall inverter design methodology developed under this project. This methodology can be applied to the design of inverters of this type for a variety of applications and operating conditions.

Steady-state performance measurements with the breadboard inverter and the prototype centrifugal compressor covered a speed range of 4400 to 8600 rev/s, with mass flows ranging from 0.3 to 1.7 g/s and pressure ratios ranging from 1.1 to 2.2. These tests were run with air as the compressor working fluid. (The compressor design point with neon as the working fluid is 1.16 g/s at 1.71 pressure ratio. A pressure ratio of 1.71 in neon corresponds approximately to 2.1 in air.) Calculated inverter efficiencies over these tests ranged from 0.89 to 0.95, at inverter input powers ranging from 56 to 437 watts.

Several start-stop tests were performed to verify the general compatibility of the inverter and motor with the starting characteristics of self-acting tilt pad bearings. The compressor started smoothly in all cases and starting currents were modest. Upper limits on the starting current were determined through locked rotor tests, in which current drawn by the motor is measured with the rotor held stationary. For the conditions used for the start-stop tests, the locked rotor current is 2 to 3 times the measured starting current, indicating that the rotor spins up quickly enough to prevent the locked rotor current from being realized. Even so, MOSFET currents for the locked rotor condition are only 25% of the rated currents, showing that the inverter is capable of handling a locked rotor condition with a substantial safety margin.

A preliminary design was performed for an engineering model that will be developed in a future phase of the SSRB cryocooler development contract. This preliminary design effort consisted of the selection of space-qualifiable electronic components and the design of a packaging scheme that allows the inverter to be mounted directly to the compressor housing. It was verified that all of the critical switching circuit components, including the MOSFET's, have equivalents that are manufactured and screened to MIL standards. Mounting the inverter to the compressor allows the electronics to transfer heat by conduction to the compressor housing which is cooled by the spacecraft thermal bus. An engineering model based on the sizing of the breadboard will weigh approximately 2.0 kg and occupy a cylindrical envelope of 17.1 cm diameter by 10.4 cm length.

The transformer-coupled inverter and the compressor's induction motor comprise a conventional open loop drive system. Variables defining the inverter's operating condition are the switching frequency, the DC input voltage and the motor impedance. Switching frequency is set by a resistance value in a simple digital oscillator circuit. DC voltage will be controlled by a pre-regulator between the inverter and the spacecraft bus. Motor impedance is determined by the load on the compressor which will be constant for normal operation. The pre-regulator and the control electronics to provide a period of reduced frequency and voltage at start-up will be developed in conjunction with the engineering model inverter in the future phase of the on-going SSRB cryocooler contract.

With minimal control requirement, and with the simple switching circuit that the tests with the breadboard inverter convincingly demonstrated, the potential for this inverter concept to meet the long life, high reliability and high efficiency requirements of the spaceborne cryocooler application is excellent.

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1. INTRODUCTION

Cryocoolers based on the reverse-Brayton cycle can use gas bearing turboexpanders and turbocompressors to provide long life and freedom from vibration in spaceborne sensor applications. A single stage reverse-Brayton (SSRB) cryocooler is currently being developed by NASA/GSFC to provide 5 watts of cooling at 65 K for a range of space sensor applications [1]. Key components for this cooler, consisting of a single-stage turboexpander, a high effectiveness heat exchanger, a single-stage motor-driven centrifugal compressor, and an electrical drive for the motor have been developed under a series of parallel contracts. A recently awarded contract (NAS5-31281) is supporting the integration of these components into a self-contained spaceborne cryocooler This is the final report on Contract NAS5-30630, a Phase II Small Business Innovation Research (SBIR) project to develop a three-phase high frequency AC inverter to drive the compressor motor.

Design parameters for the inverter are driven by the design of the compressor motor which is described in [1]. The motor has a 0.25 inch (0.635 cm) diameter shaft with a nominal rotational speed of 8000 rev/s. The projected power requirement for the compressor is 175 watts. The motor is a three-phase solid rotor induction motor, designed with stator coils of a low number of turns of moderately heavy gauge wire to ease the conduction of heat from the coils. The low number of turns, combined with the small size of the motor, results in a low operating AC voltage, nominally 15 volt-rms, with high current, nominally 8 amp-rms per phase. Design objectives for the inverter are high efficiency (90 to 95%) and low harmonic content at this nominal design condition. An additional requirement is that the inverter components be sized to carry the starting current drawn by the induction motor. At zero speed, the electrical impedance of an induction motor is a minimum, resulting in starting currents that can significantly exceed the operating current.

The inverter design goals of high efficiency and low harmonic content are based on the general objective of keeping the electrical power demand of the cryocooler as low as possible. The importance of this for spaceborne sensor applications is well documented [2] Harmonics in the inverter output should be avoided to whatever extent possible because they contribute losses in the motor without contributing useful output, lowering the efficiency of the motor.

Power inverters, known as variable speed motor drives, are available commercially from many suppliers. These are not well suited to the present application. The highest frequency commercial inverters tend to have rectangular waveforms with high harmonic content. They are also not optimized for the low voltage-high current character of the compressor motor. Pulse width modulation (PWM) is used to eliminate higher harmonics in some advanced commercial inverters. PWM, however, relies on microprocessor control, and computation time generally limits output frequencies to 200 Hz and lower.

Based on the above realities, a search of commercially available inverters failed to turn up anything suitable, establishing the need to develop a high frequency inverter specially tailored to the requirements of the SSRB compressor motor. Under the present project, an inverter concept particularly suited to these requirements has evolved from the invention demonstrated in Phase I [3]. This concept is a unique embodiment of a transformer-coupled inverter which uses six toroidal transformers and twelve MOSFET switches connected in a ring topology. AC waveforms in which all harmonics below the eleventh are eliminated are assembled at the transformer secondary coils from square waves that are generated by switching the primary coils between the supply voltage and ground.

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Various configurations of transformer-coupled inverters have been described in the literature [4-10], but the ring topology used here, which may be an optimum arrangement of six transformers and twelve switches, appears novel. The present ring topology is a natural extension of the rotating field inverter (RFI) of Phase I, which used a single multi-coil transformer. The ring topology reflects the interconnection of the coils in the RFI transformer. The use of six separate transformers came about in an effort to reduce the RFI's high magnetizing current by eliminating its air gap.

This report describes the successful development and demonstration of a breadboard version of the six-transformer ring-topology inverter that was sized for the above specification. The general design methodology, described in detail in Section 2, is not limited to the present cryocooler application. It can be used to size an inverter of this type for any set of specifications. Section 2 also describes the electronic details of the MOSFET switching circuit, control issues for the inverter, and packaging of the breadboard. It should be emphasized that the electronics are exceedingly simple and that control of the output waveforms is fully open loop, contributing further to the simplicity and potential high reliability of the design.

Test results with the breadboard inverter are presented in Section 3. The breadboard showed an efficiency of 95% while driving a prototype compressor at frequencies and power levels in excess of 8 kHz and 300 watts. Calorimeter measurements which verify the relations used to predict inverter losses are described in Section 3. Also given in Section 3 are the results of start-up tests with tilting pad bearings and locked-rotor current measurements. The locked rotor results show that the maximum possible starting currents are well below the current ratings of the MOSFET switches. Finally, a preliminary design for an engineering model inverter is described in Section 4. This engineering model is scheduled to be fabricated and integrated into the SSRB cryocooler in a future phase of Contract NAS5-31281. Conclusions and recommendations are summarized in Section 5.

The period of performance for Phase II was May 1989 through May 1991. Max Gasser was the NASA/GSFC Technical Monitor. Dr. Javier Valenzuela was the Principal Investigator and Dr. John A. McCormick served as Project Engineer. Technical contributors at Creare were M. Ackerson, W. Affleck, M. Bagley, S. Childs, M. Drabick, D. Falkowski, D. King, H. Sixsmith, W. Swift, and J. White.

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2. DESIGN OF BREADBOARD INVERTER

2.1 Inverter Concept and Theory of Operation

The present high frequency power inverter concept has evolved from the rotating field inverter that was studied in Phase I [1]. Although its output waveform quality was excellent, high magnetizing currents made the rotating field inverter unsuitable for the power levels of the SSRB compressor. That problem is avoided in the present concept, which uses six small toroidal transformers in place of the single large transformer of the rotating field inverter. A thorough description of the rotating field inverter is given in [1]. That description will not be repeated here since it isn't needed to understand the present concept.

Figure 1 shows a simplified overall schematic of the six-transformer inverter that has been developed during Phase II. The primary coils of the six toroidal transformers are connected in series in a ring. These coils are sequentially energized from the DC bus at voltage V_o through the six pairs of MOSFET transistor switches which supply chopped voltage signals V_{p1} through V_{p6}. The secondary coils, located on the inside of the ring of transformers provide a three-phase Y-connected AC output consisting of line-to-neutral voltages V_{s1}, V_{s2} and V_{s3}. Each of these phase voltages can be seen to be derived from a series connection of the secondary coils of two diametrically opposed toroids. This is basically the same arrangement of primary and secondary coils that had been wound on a single large toroidal core in the original rotating field concept.

The timing pattern of the MOSFET switches on the primary side that provides a high quality AC output at the secondary is similarly an outgrowth of the original rotating field concept. One way to view the pattern that will now be described is as a rotating pattern of primary coil energization that sequentially energizes the three secondary phases.

The MOSFET switches generate the input voltages V_{p1} through V_{p6} by alternately switching the primary leads between V_0 and ground. These input voltages in turn produce voltage waveforms across the primary coils that are transformed to the secondary coils. Extensive experimentation has led to the pattern represented by the six V_p waveforms shown in Figure 2. Each V_p waveform follows the pattern of the logic signals that trigger the IR2110 bridge drivers to switch the MOSFET's on and off. These logic signals, denoted as Q1 through Q6 with complementary signals $\overline{Q1}$ through $\overline{Q6}$, are generated by the six cascaded D-type flip flop elements shown at the top of Figure 1. A timing chip (not shown) provides the clock signal that triggers the flip flops. Each Q signal, and consequently each V_p waveform, is a square wave whose period equals 12 clock periods. The inverter output waveform is constructed from these V_p waveforms and therefore has the same period. The inverter output frequency is thus one-twelfth the clock frequency. Setting of the clock frequency through a potentiometer adjustment in the timing chip circuit sets the inverter frequency. The clock, Q and $\overline{Q}$ signals are shown in Figure 3.

Each V_p waveform is high (V_0) for six clock periods and low (ground) for the next six clock periods. Phase delays between successive V_p waveforms are seen to alternate between three clock periods and one clock period. Referring to Figure 1, the delay is three clock periods between the V_p leads across the transformers labeled a1, a2 and a3, and one clock period between the leads across transformers b1, b2 and b3.

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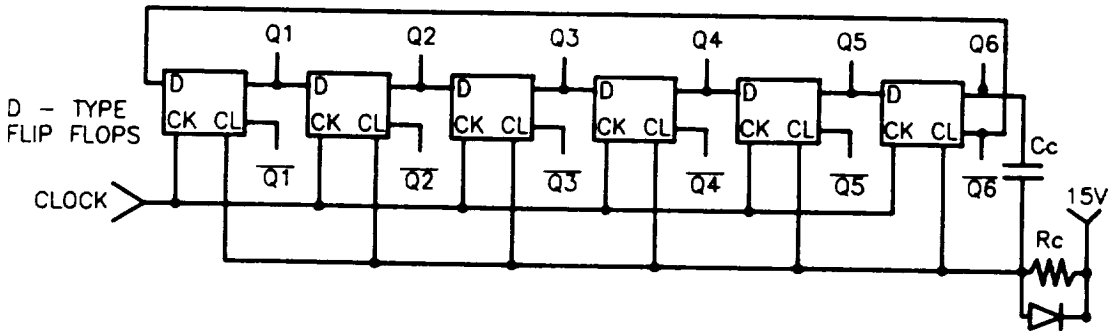

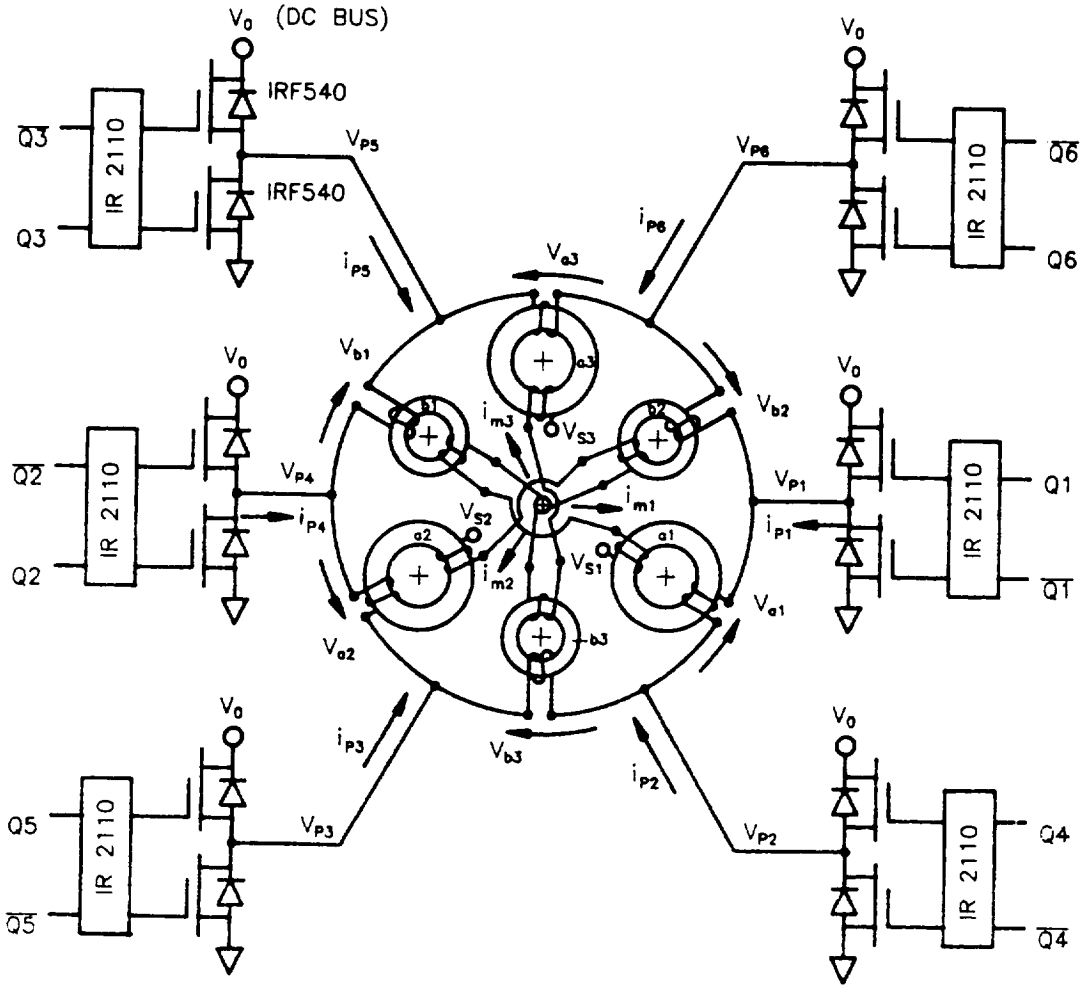

Figure 1. SIMPLIFIED SCHEMATIC OF INVERTER

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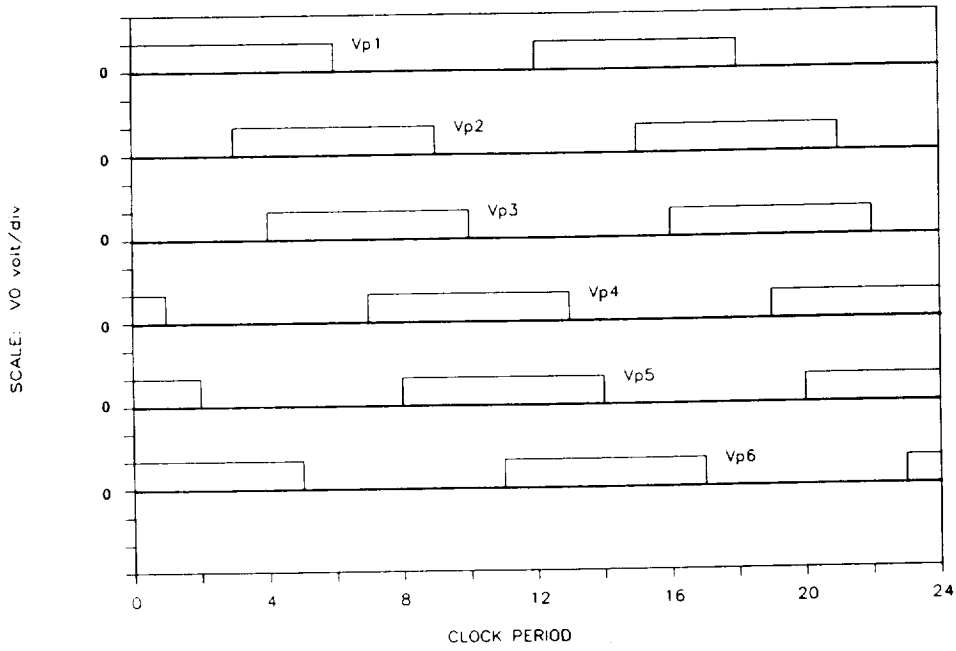

Figure 2. VOLTAGE WAVEFORMS AT PRIMARY COIL LEADS: V_{p1}, V_{p2}, V_{p3}, V_{p4}, V_{p5}, V_{p6}

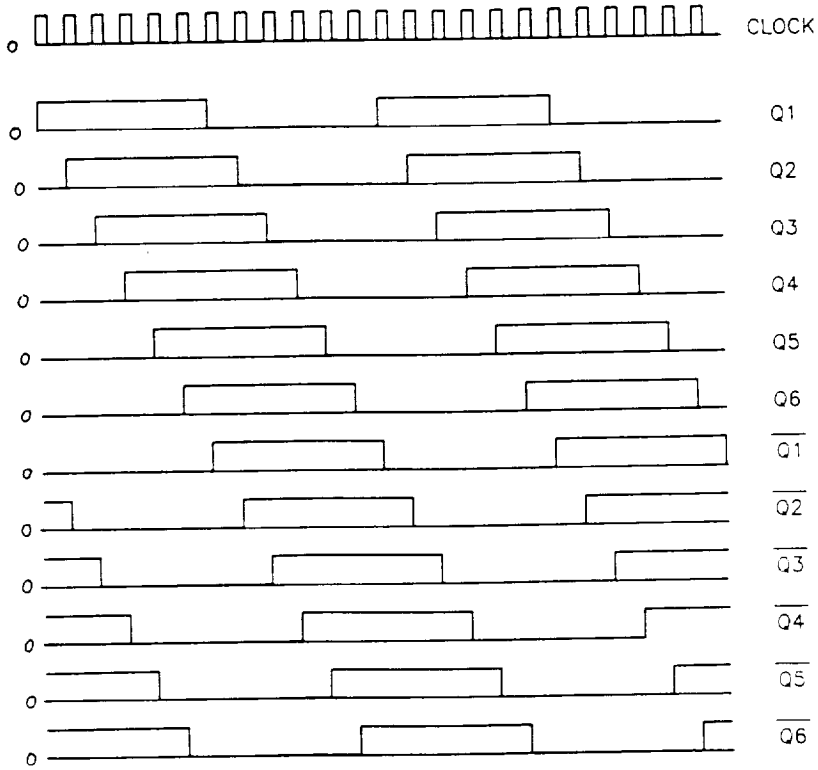

Figure 3. LOGIC OUTPUT SIGNALS FROM D FLIP-FLOPS

In working from the V_p waveforms to the eventual secondary output waveforms, the next step is to examine the primary coil waveforms V_{a1}, V_{a2}, V_{a3}, V_{b1}, V_{b2} and V_{b3} formed by the differences between adjacent V_p waveforms:

$$V_{a1} = V_{p1} - V_{p2} \qquad V_{b1} = V_{p5} - V_{p4}$$

$$V_{a2} = V_{p3} - V_{p4} \qquad V_{b2} = V_{p1} - V_{p6}$$

$$V_{a3} = V_{p5} - V_{p6} \qquad V_{b3} = V_{p3} - V_{p2}$$

These are shown in Figure 4. Each primary coil waveform consists of alternating positive and negative square pulses of height V_0. The width of these pulses is equal to the phase delay between the two V_p waveforms across the coil, 3 clock periods for transformers a1, a2 and a3 and one clock period for transformers b1, b2 and b3. With one-third the voltage pulse width, the peak magnetic flux in the "b" transformers is one-third that in the "a" transformers. The "b" transformers can thus have a substantially smaller core cross section as Figure 1 indicates.

The line to neutral output voltage V_{s1} is the sum of the secondary coil voltages for transformers a1 and b1. Output voltages V_{s2} and V_{s3} are similarly formed from transformer pairs (a2, b2) and (a3, b3). Assuming ideal transformers, these output voltages are given by

$$V_{s1} = (N_{sa}/N_{pa})\, V_{a1} + (N_{sb}/N_{pb})\, V_{b1}$$

$$V_{s2} = (N_{sa}/N_{pa})\, V_{a2} + (N_{sb}/N_{pb})\, V_{b2}$$

$$V_{s3} = (N_{sa}/N_{pa})\, V_{a3} + (N_{sb}/N_{pb})\, V_{b3}$$

where N_{pa} and N_{pb} are the numbers of primary turns for the "a" and "b" transformers, and N_{sa} and N_{sb} are the numbers of secondary turns. The V_s waveform is a superposition of the three clock period wide pulses of the V_a waveform with the one clock period wide pulses of the V_b waveform.

When a Y-connected three phase load, representing the compressor motor, is connected to the secondary as shown in Figure 5, the line-to-neutral voltages V_{m1}, V_{m2} and V_{m3} across the load impedances are formed according to

$$V_{m1} = (2V_{s1} - V_{s2} - V_{s3}) / 3$$

$$V_{m2} = (2V_{s2} - V_{s3} - V_{s1}) / 3 \qquad (1)$$

$$V_{m3} = (2V_{s2} - V_{s3} - V_{s1}) / 3$$

Note that these are independent of the load impedance. Figure 6 shows the V_s and resulting V_m waveforms for the three phases. Figure 7 shows the details of typical V_s and V_m waveforms. The combination of the three relatively sharp edged V_s waveforms yields V_m waveforms that are substantially smoother by virtue of a greater number of steps. By properly selecting the V_m step heights, which are determined by the turns ratios, the V_m waveshape can be made to closely approximate a sine wave.

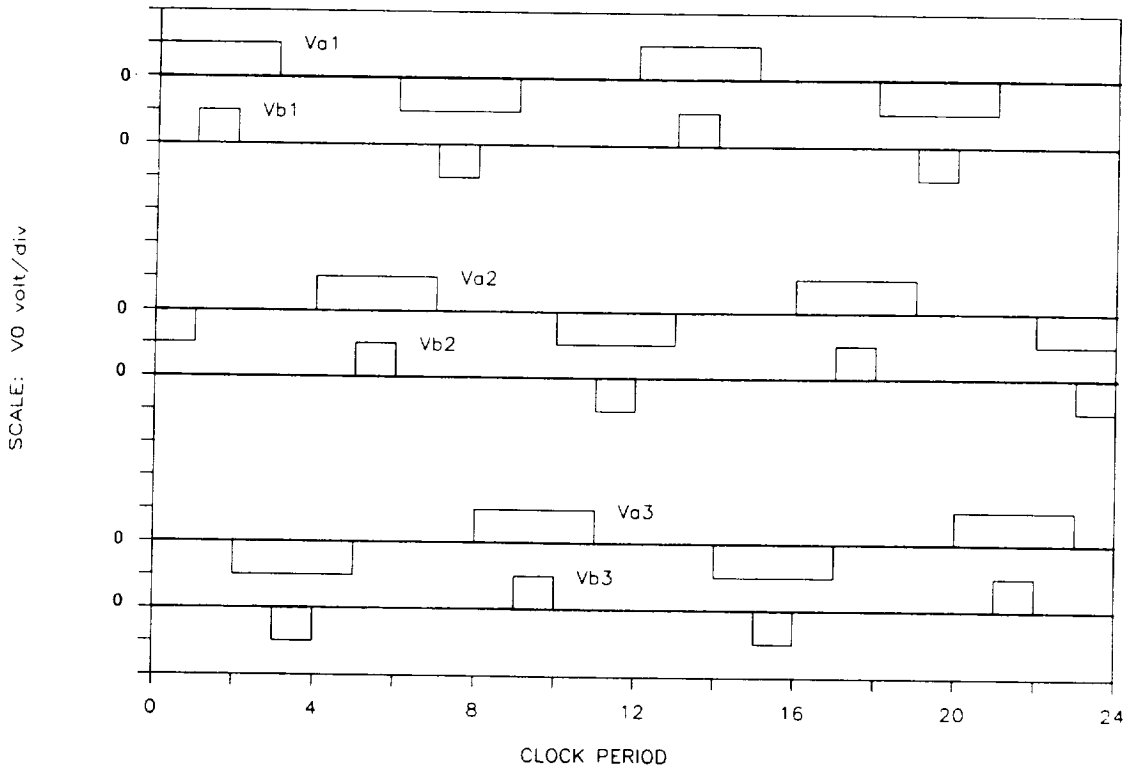

Figure 4. VOLTAGE WAVEFORMS ACROSS PRIMARY COILS: V_{a1}, V_{b1}, V_{a2}, V_{b2}, V_{a3}, V_{b3}

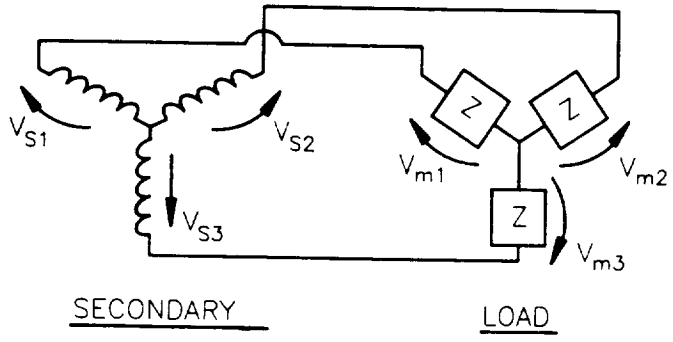

Figure 5. Y-CONNECTED SECONDARY AND LOAD

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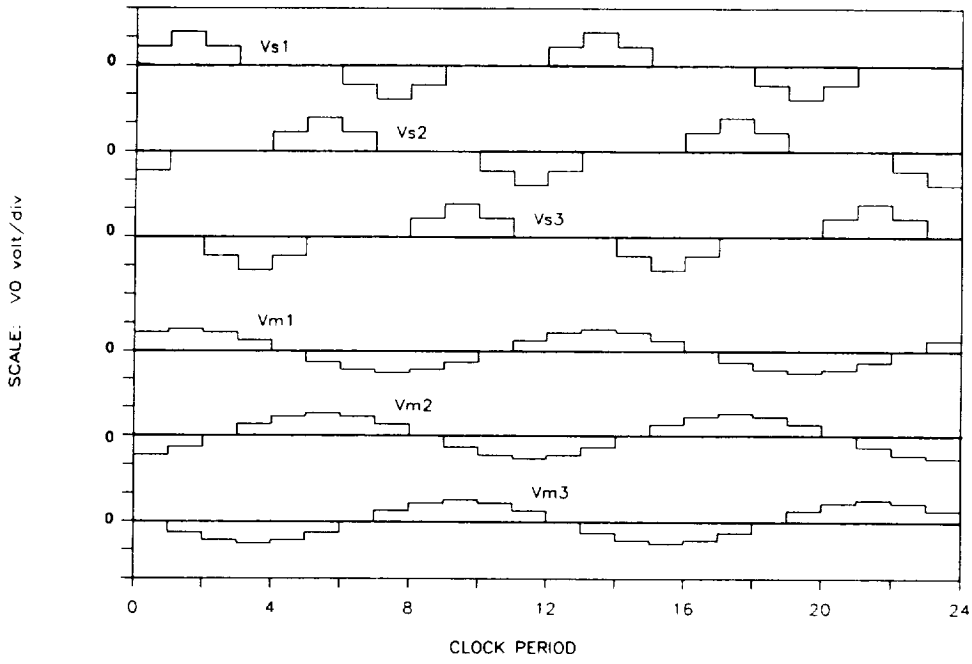

Figure 6. VOLTAGE WAVEFORMS ACROSS SECONDARY COILS AND LOAD IMPEDANCES, WITH TURNS RATIOS N_{sa}/N_{pa} = 2/3 AND N_{sb}/N_{pb} = 1/2: V_{s1}, V_{s2}, V_{s3}, V_{m1}, V_{m2}, V_{m3}

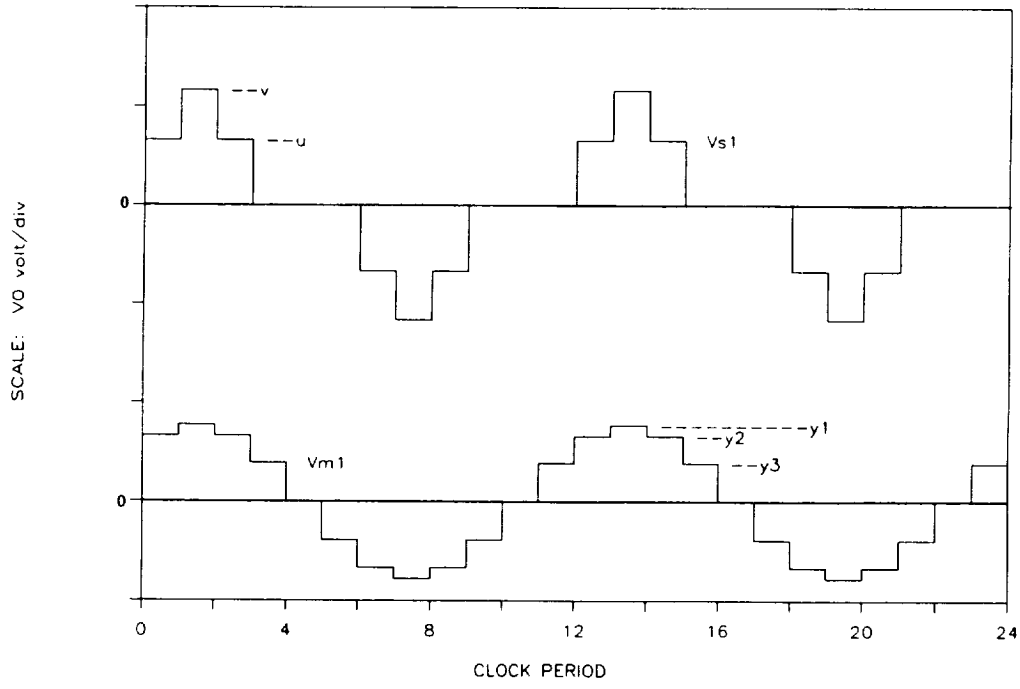

Figure 7. SECONDARY COIL AND LOAD VOLTAGE WAVESHAPES FOR ONE PHASE: WITH TURNS RATIOS N_{sa}/N_{sp} = 2/3 AND N_{sb}/N_{pb} = 1/2: V_{s1}, V_{m1}

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Criteria for selecting the turns ratios can be derived from an examination of the voltage levels at the steps of the V_s and V_m waveforms. In the V_s waveform shown in Figure 7, the voltage levels at the two steps are

$$u = (N_{sa}/N_{pa})\, V_0 \tag{2}$$

$$v = [(N_{sa}/N_{pa}) + (N_{sb}/N_{pb})]\, V_0 \tag{3}$$

reflecting superposition of the V_a and V_b waveforms. Voltage levels y1, y2 and y3 at the steps of the V_m waveform as shown in Figure 7 are related to u and v through Equations (1):

$$y1 = 2v/3 \tag{4}$$

$$y2 = u \tag{5}$$

$$y3 = v/3 \tag{6}$$

Voltage level y1 is the amplitude of the V_m waveform, which will be denoted by V_{m0}:

$$y1 = V_{m0} \tag{7}$$

It can be shown through a straightforward Fourier series analysis of the stepped V_m waveform that the stepped shape best approximates a sine wave when y2 and y3 are related to y1 through

$$y2 = y1 \sin 60° \tag{8}$$

$$y3 = y1 \sin 30° \tag{9}$$

In practice, all harmonics of the inverter frequency below the eleventh are eliminated from the V_m waveform when Eqs. (8) and (9) are satisfied. Since sin 30° = 0.5, Eq. (9) is automatically satisfied by Eqs.(4) and (6). Equation (8) defines a ratio between the turns ratios of the "a" and "b" transformers. First, from Eqs (8), (4) and (5):

$$y2/y1 = \sin 60° = (3/2)\, u/v$$

The ratio of the "a" and "b" turns ratios is obtained by substituting from Eqs. (2) and (3) for u and v:

$$(N_{sb}/N_{pb}) / (N_{sa}/N_{pa}) = 0.7321 \tag{10}$$

Whether or not the transformer designs satisfy Eq. (10), the output voltage amplitude V_{m0} is determined by the actual turns ratios and the input DC voltage V_0 according to Eqs. (7), (4) and (3):

$$V_{m0} = (2/3)\, [(N_{sa}/N_{pa}) + (N_{sb}/N_{pb})]\, V_0 \tag{11}$$

Eqs. (10) and (11) can be combined to yield these expressions for the most favorable turns ratios in terms of V_{m0}/V_0:

$$N_{sa}/N_{pa} = 0.8660\, V_{m0}/V_0 \tag{12}$$

$$N_{sb}/N_{pb} = 0.6340\ V_{m0}/V_0 \qquad (13)$$

These last two equations should be applied cautiously since V_{m0}/V_0 is truly determined only by the sum of the two turns ratios through Eq. (11). Eqs. (12) and (13) are only valid when the ratio of N_{sb}/N_{pb} to N_{sa}/N_{pa} is exactly 0.7321, providing the best approximation to a sine wave that is possible with the stepped V_m waveform.

Having fully determined the relations defining voltage levels and waveshapes throughout the inverter, the next step in describing the concept is to analyze the currents. Once this is accomplished, all information needed to size the transformers and switching transistors is available. The analysis of the currents will begin at the load and work back to the primary leads.

Each of the phase loads shown in Figure 5 can be modeled as a resistance R in parallel with an inductance L. Figure 8 shows the load elements and currents for the three phases. The currents are obtained from the known V_m waveforms as follows:

$$i_r = V_m / R$$

$$i_x = (1/X) \int V_m\, d(\omega t)$$

$$i_m = i_r + i_x$$

where t is time, ω is the angular frequency and $X = \omega L$ is the reactance. These equations hold for each phase but the phase subscripts have been omitted for conciseness. It should be noted that the integration process will smooth out the steps in the V_m waveform, making the i_x waveform appear as nearly a pure sine wave. The shape of the resultant current waveform i_m depends only on the ratio R/X which represents the power factor angle θ according to

$$R/X = \tan \theta$$

Figure 9 shows the calculated i_r, i_x and i_m waveforms for phase 1 with $\theta = 60°$, which is the nominal power factor angle for the compressor motor. The saw tooth irregularities in i_m follow from the superposition of the stepped i_r waveform with the smooth i_x waveform. This characteristic is borne out in the actual inverter, both when driving a dummy reactive and resistive load and when driving the compressor motor. In Figure 10 the calculated i_m and V_m waveforms are shown for all three phases with $\theta = 60°$.

The resultant load currents i_{m1}, i_{m2} and i_{m3} flow through the secondary coils of the inverter as indicated on the Figure 1 schematic. According to the ideal transformer model the currents in the primary coils are:

$$i_{a1} = (N_{sa}/N_{pa})\, i_{m1} \qquad i_{b1} = (N_{sb}/N_{pb})\, i_{m1}$$

$$i_{a2} = (N_{sa}/N_{pa})\, i_{m2} \qquad i_{b2} = (N_{sb}/N_{pb})\, i_{m2}$$

$$i_{a3} = (N_{sa}/N_{pa})\, i_{m3} \qquad i_{b3} = (N_{sb}/N_{pb})\, i_{m3}$$

From these the currents in the primary leads are obtained according to

$$i_{p1} = i_{b2} + i_{a1} \qquad i_{p2} = -\, i_{a1} - i_{b3}$$

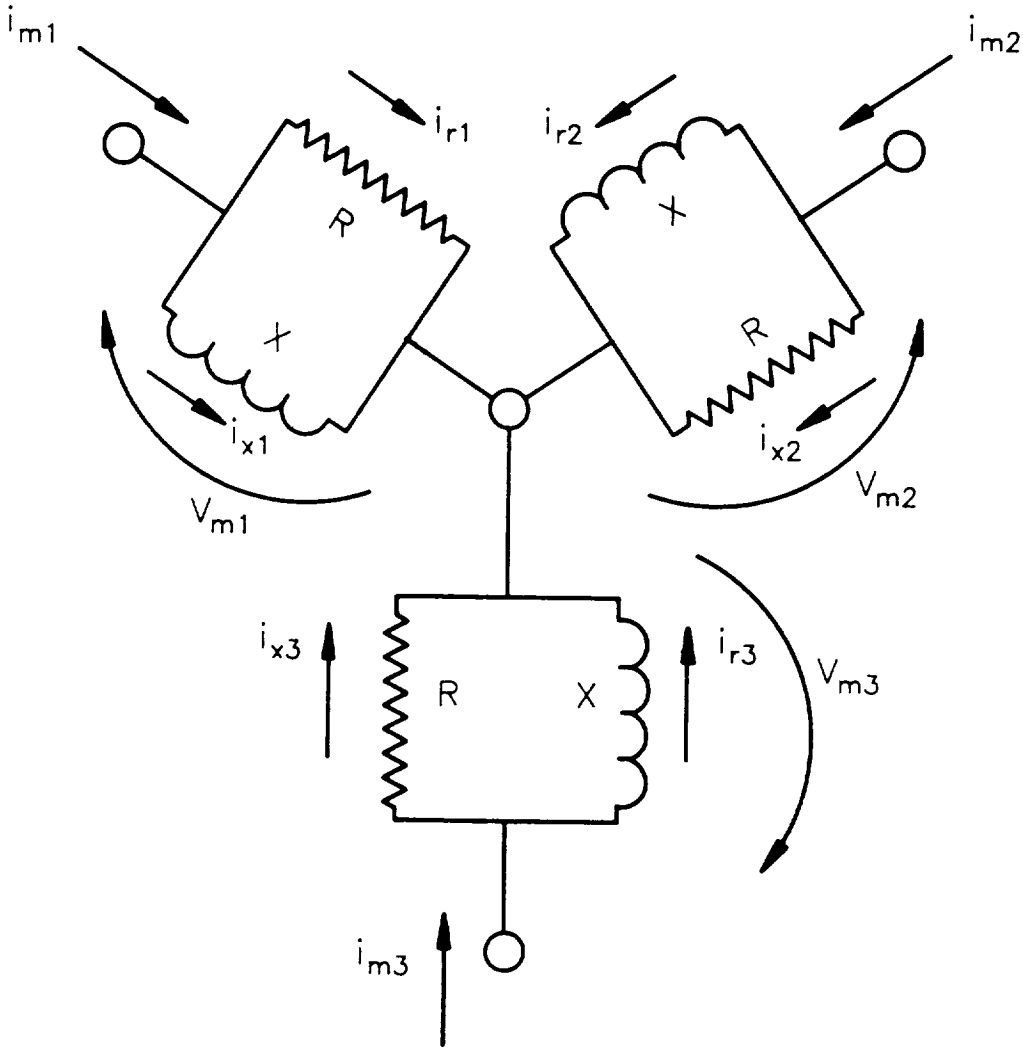

Figure 8. Y-CONNECTED SECONDARY LOAD

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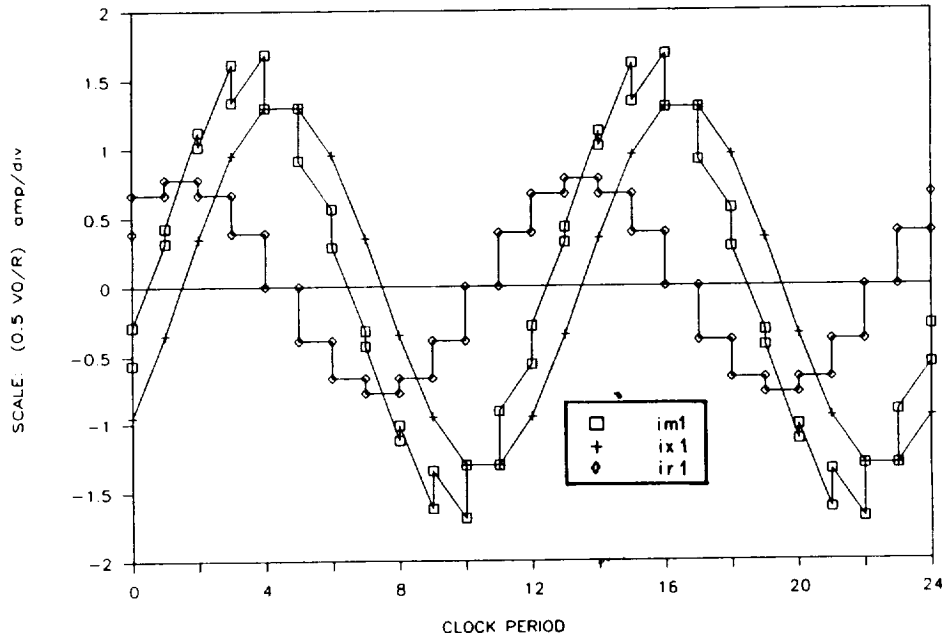

Figure 9. COMPONENTS OF LOAD CURRENT WAVEFORM FOR ONE PHASE WITH 60° POWER FACTOR AT LOAD: i_{r1} (RESISTIVE), i_{x1} (REACTIVE), i_{m1} (TOTAL)

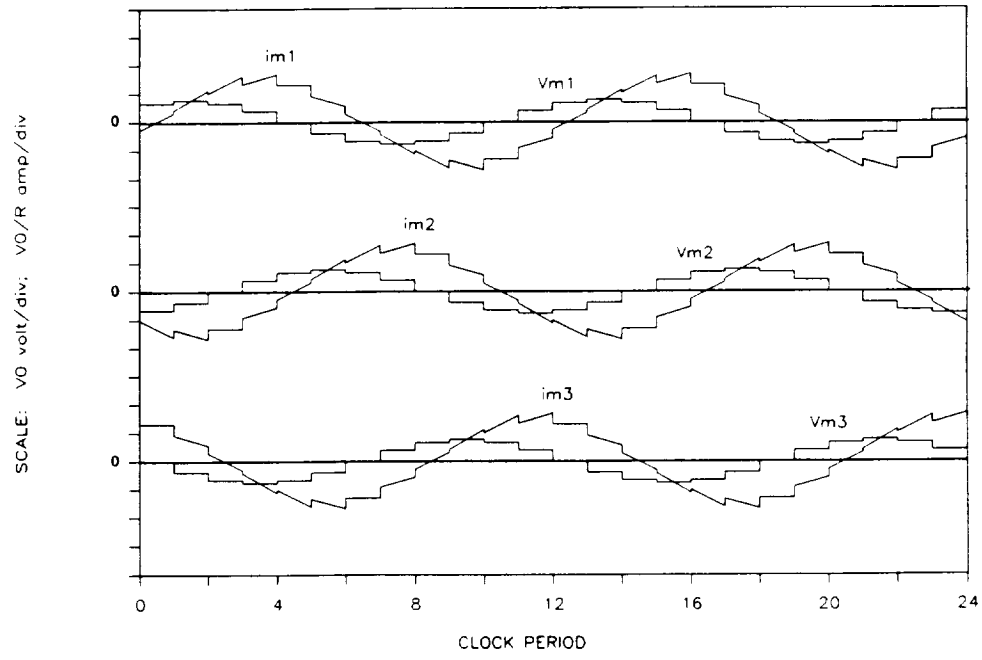

Figure 10. LOAD VOLTAGE AND CURRENT WAVEFORMS FOR THREE PHASES WITH 60° POWER FACTOR AT LOAD: V_{m1}, i_{m1}, V_{m2}, i_{m2}, V_{m3}, i_{m3}

$i_{p3} = i_{b3} + i_{a2}$ $\qquad$ $i_{p4} = -i_{a2} - i_{b1}$

$i_{p5} = i_{b1} + i_{a3}$ $\qquad$ $i_{p6} = -i_{a3} - i_{b2}$

Figure 11 shows the six i_p waveforms obtained from the i_m waveforms of Figure 10.

The portion of the i_p waveform where the corresponding V_p waveform is at V_0 represents the current flowing from the DC supply to the inverter through that lead. By adding up these portions for the six i_p waveforms, the total current flowing from the DC supply is obtained. Figure 12 shows this total supply current calculated for the i_p waveforms of Figure 11. It is seen to consist of a DC component of approximately 0.9 V_0/R amp, a saw tooth ripple at the clock frequency and a slight third harmonic ripple. The DC component of this supply current, which will be denoted as i_0, represents the input power W_0 to the inverter according to

$$W_0 = i_0 V_0$$

The total output power W_m delivered to the three load resistors is:

$$W_m = \frac{3}{2} V_{m0}^2/R$$

In the present analysis $W_m = W_0$ since inverter loss is not included, resulting in $i_0 = W_m/V_0$. From Eq (1) with $N_{sa}/N_{pa} = 2/3$ and $N_{sb}/N_{pb} = 1/2$, $V_{m0} = 0.778\ V_0$, providing $i_0 = 0.908\ V_0/R$ as shown by Figure 12.

The sawtooth ripple on the input current in Figure 12 is a 12th harmonic of the inverter frequency. This is readily eliminated in practice by placing a small filter capacitor (2.2 microfarad) across each pair of MOSFET switches between V_0 and ground. The unfiltered 12th harmonic ripple is associated with the phasing between the V_p and i_p waveforms. The amplitude of this ripple can be shown to be a maximum when the load is purely reactive (V_p and i_p are 90° out of phase) and a minimum when the load is purely resistive (V_p and i_p are in phase).

The difference in height between the adjacent sawtooth peaks in Figure 12 represents the amplitude of the third harmonic ripple that would remain after the sawtooth is filtered out. This can be seen to be 1 to 2% of the DC current, making the resultant disturbance fed to the 28 volt DC bus by the inverter a 24 kHz current ripple whose amplitude is 1 to 2% of the DC current. The third harmonic ripple is caused by slight asymmetry in the i_m waveform that results from superposition of the stepped resistive current waveform with the smooth reactive current waveform.

The preceding analysis has defined all voltage and current waveforms within the inverter. To summarize the results, it is useful to treat the V_m, i_m, i_a, i_b and i_p waveforms as pure sine waves with amplitudes V_{m0} , i_{m0} , i_{a0} , i_{b0} and i_{p0}. In terms of V_0 and the turns ratios, the waveform amplitudes are

$$V_{m0} = (2/3)\ [(N_s/N_{pa}) + (N_{sb}/N_{pb})]\ V_0 \qquad (14)$$

$$i_{m0} = V_{m0} / (R \cos \theta) \qquad (15)$$

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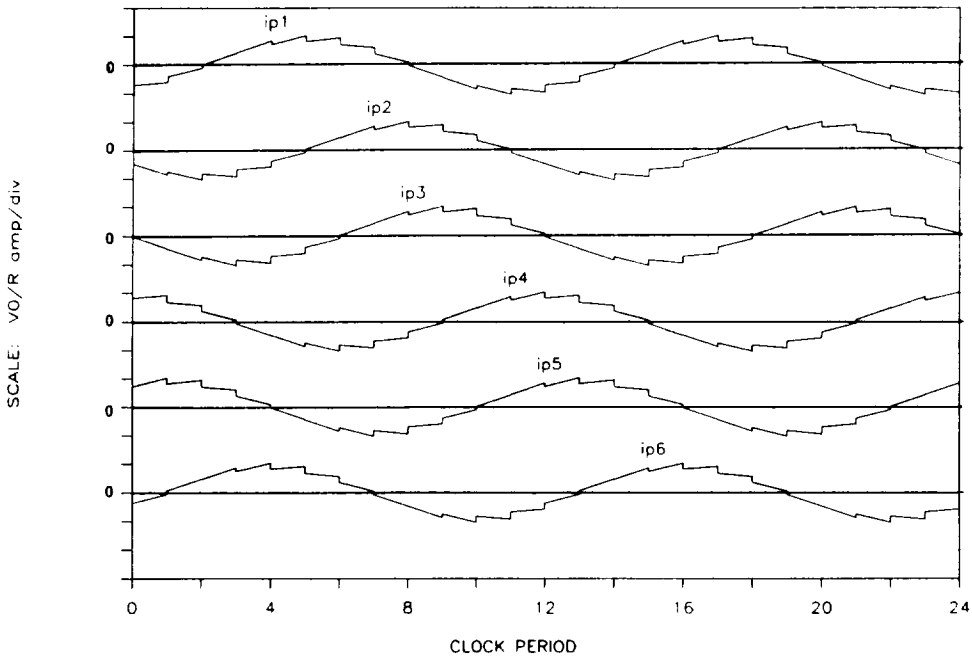

Figure 11. CURRENT WAVEFORMS FOR PRIMARY COIL LEADS WITH 60° POWER FACTOR AT LOAD: i_{p1}, i_{p2}, i_{p3}, i_{p4}, i_{p5}, i_{p6}

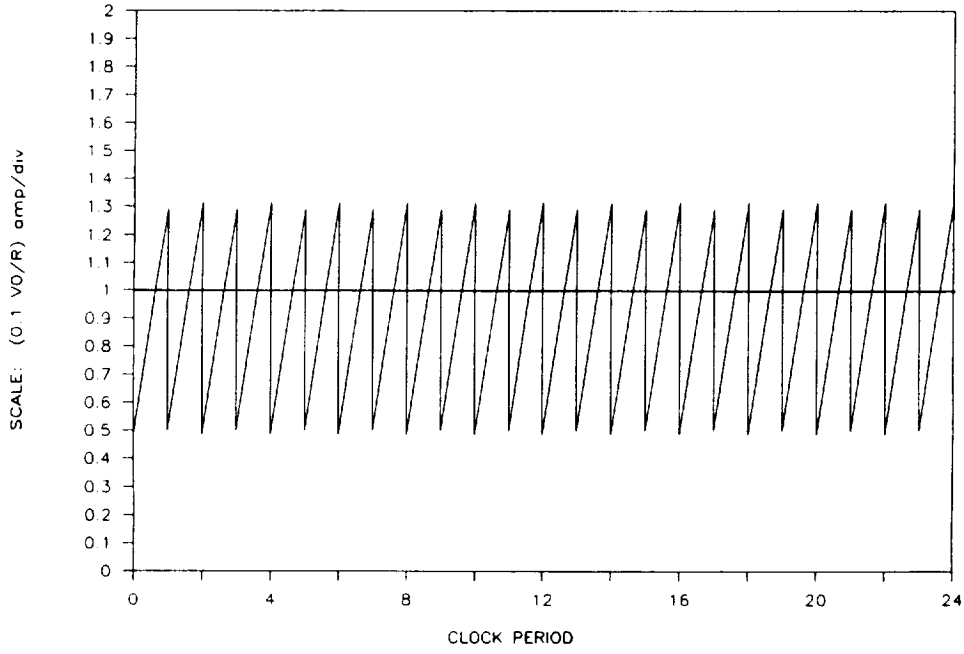

Figure 12. TOTAL CURRENT TO INVERTER FROM DC BUS WITH 60° POWER FACTOR AT LOAD

$$i_{a0} = (N_{sa}/N_{pa})\, i_{m0} \tag{16}$$

$$i_{b0} = (N_{sb}/N_{pb})\, i_{m0} \tag{17}$$

$$i_{p0} = (i_{a0}^2 + i_{b0}^2 - i_{a0}\, i_{b0})^{\frac{1}{2}} \tag{18}$$

The relation for i_{p0} follows from the superposition of an i_a and an i_b waveform to form each i_p waveform. It can be seen from the preceding analysis of the current waveforms that each i_p is formed from an i_a and an i_b that are 60° out of phase. The current amplitudes determine the resistive losses in the transformer coils and MOSFET's. The input DC current i_0 is determined by the input power W_0 according to

$$i_0 = W_0/V_0 \tag{19}$$

W_0 is the sum of the output power W_m and the inverter losses, with W_m given by

$$W_m = (3/2)\, V_{m0}^2/R \tag{20}$$

Finally, to provide the V_m waveform that best approximates a sine wave, the turns ratios should be selected according to

$$N_{sa}/N_{pa} = 0.8660\, V_{m0}/V_0 \tag{21}$$

$$N_{sb}/N_{pb} = 0.6340\, V_{m0}/V_0 \tag{22}$$

2.2 Inverter Specification

The inverter specification is based on the preliminary design point and efficiency target for the SSRB compressor and motor [1]. This present specification is as follows:

Output power	$W_m = 175$ watt
Input DC voltage	$V_0 = 28$ volt
Output AC voltage - line to neutral	$V_{m0} = 21.2$ volt (15 volt-rms)
Output frequency	f = 8 kHz
Power factor	$\cos\theta = 0.5$
Target Efficiency	$\eta_{inv} = W_m/W_0 = 0.90$
Starting Condition	$V_0 = 14$ volts f = 4 kHz

From the above voltage levels and the ideal turns ratios are:

$$N_{sa}/N_{pa} = 0.8660 \times 21.2 \div 28 = 0.656$$

$N_{sb}/N_{pb} = 0.6340 \times 21.2 \div 28 = 0.480$

These are rounded to the practically attainable values

$N_{sa}/N_{pa} = 2/3$

$N_{sb}/N_{pb} = 1/2$

which for $V_0 = 28$ volts yields from the Equation (14):

$V_{m0} = 2/3 \times (2/3 + 1/2) \times 28 = 21.8$ volts

The equivalent load resistance R, for one phase, can be calculated from Eq. (20):

$R = 3/2 \times 21.8^2 \div 175 = 4.07$ ohm

The current amplitudes can now be calculated from Equations (15) - (18):

$i_{m0} = 21.8 \div (4.07 \times 0.5) = 10.7$ amp

$i_{a0} = 2/3 \times 10.7 = 7.13$ amp

$i_{b0} = 1/2 \times 10.7 = 5.35$ amp

$i_{p0} = (7.3^2 + 5.35^2 - 7.3 \times 5.35)^{\frac{1}{2}} = 6.43$ amp

Assuming the efficiency is 0.90, the DC current supplied by the bus at 28 volts would be:

$i_0 = 175 \div 0.90 \div 28 = 6.94$ amp

These current amplitudes determine the resistive loss in the transformers and MOSFET's, whose designs for the breadboard inverter are discussed in the next two sections. Voltage and frequency determine the magnetic field which the transformers must be sized to carry. Since the existing breadboard compressor uses a primitive impeller design which has not been optimized, its compressor efficiency is much lower than the 40% target value for the SSRB. As a result the breadboard inverter must supply substantially more power than 175 watts in driving the breadboard compressor at the SSRB design point flow and pressure ratio. This additional power increases the current in the transformers and MOSFET's from the above values, resulting in higher resistive loss and lower inverter efficiency. To enable the breadboard inverter to comfortably handle W_m values up to 500 watts during testing, MOSFET's were selected with conservative current ratings and two were used in parallel for each switch. The influence of operating condition on inverter efficiency is discussed extensively in Sections 2.5 and 3.2.3. Voltage regulation and start-up is discussed in Section 2.7.

2.3 Sizing of Transformers

Ferrite toroids were chosen for the transformer cores of the breadboard inverter, both for design conservatism and for convenience. Ferrites are dense homogeneous ceramic structures made by mixing iron oxide (Fe_2O_3) with oxides or carbonates of one or more metals

such as manganese, zinc, nickel or magnesium. They are pressed, then fired in a kiln at 2000° F, and machined as needed to meet various operational requirements. Ferrites have inherently low core losses and high permeability at the 8 kHz design point frequency. They are inexpensive and readily available in a wide range of off the shelf sizes. Their main disadvantage relative to magnetic metals is their relatively low saturation flux density, typically around 0.4 tesla.

Ferrite cores are available in a variety of geometries. The toroid is the most efficient magnetically, due to the absence of an air gap and a uniform cross-sectional area. Geometries other than the toroid, tend to be designed for bobbin wound coils and for convenient mounting to PC boards. These are not important concerns at this stage of the inverter development. Given the present high current mode of operation, the transformer designs are driven, as is discussed below, to coils consisting of small numbers of turns of heavy gauge wire. Such coils have proven to be easily accommodated by the toroidal geometry.

To describe the process used in sizing the cores and coils and the resulting designs, the magnetic field will first be analyzed using Faraday's and Ampere's Laws. This will provide relations for the minimum number of primary turns and the minimum core cross-section based on a maximum allowable flux density. The selected coil and core designs which satisfy these constraints will then be shown. Finally the losses will be analyzed to demonstrate the suitability of the selected designs.

From Faraday's Law, the magnetic flux in the "a" and "b" transformer cores is determined by the primary coil voltage waveforms V_a and V_b according to

$$\phi_a = (1/N_{pa}) \int V_a \, dt$$

$$\phi_b = (1/N_{pb}) \int V_b \, dt$$

The integration is readily carried out for the waveforms in Figure 4 resulting in the peak values

$$\phi_{a0} = V_0 / (8 \, f \, N_{pa})$$

$$\phi_{b0} = V_0 / (24 \, f \, N_{pb})$$

For the same number of turns, the "b" transformers carry one-third the flux of the "a" transformers. This is because the square pulses comprising the V_b waveform are one-third the length of those comprising the V_a waveform. Figure 13 shows the geometry of the toroidal core. Through application of Ampere's Law to the circular path at radius r, it can be shown that the flux density B varies inversely with r according to

$$B(r) = B_{max} \, D_i / (2r)$$

where B_{max} is the maximum flux density. An expression for the flux in terms of B_{max} is obtained by integrating this expression over the core cross section:

$$\phi = (h \, D_i/2) \, B_{max} \ln (D_0/D_i)$$

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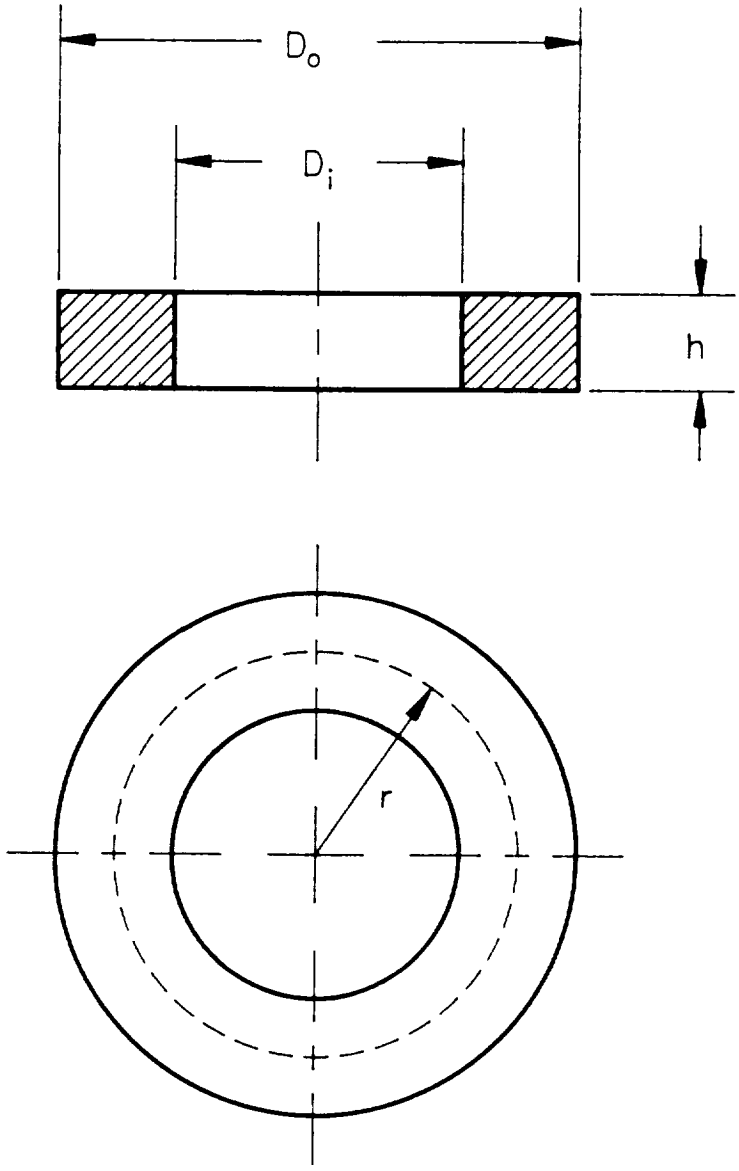

Figure 13. GEOMETRY OF TOROIDAL CORE

Equivalently

$$\phi = \beta A_{core} B_{max}$$

where

$$\beta = [\ln (D_0/D_i)] / (D_0/D_i - 1)$$

and A_{core} is the cross sectional area. Equating this last expression for ϕ with the preceding expressions for ϕ_{a0} and ϕ_{b0} provides relations that can be used directly to size the cores:

$$(\beta A_{core})_a N_{pa} = V_0 / (8 f B_{max})$$
$$(\beta A_{core})_b N_{pb} = V_0 / (24 f B_{max})$$

To keep operating flux densities safely below saturation, a nominal B_{max} of 0.25 tesla has been used to guide the design process. If B_{max} is kept safely below saturation at the design point, there is room to use a higher value of V_0/f during startup if needed. For V_0 = 28 volt, f = 8000 Hz and $B_{max} \leq 0.25$ tesla, these sizing relations give

$$(\beta A_{core})_a N_{pa} \geq 17.50 \text{ cm}^2$$
$$(\beta A_{core})_b N_{pb} \geq 5.83 \text{ cm}^2$$

Clearly, for minimum size and weight, it is desirable that these N_p-core area products be as close to the minimum values as practical. If the minimum N_p-core area products are exceeded by the design, the operating B_{max} value simply falls below 0.25 tesla, potentially reducing the core loss. This would in most cases be at the expense of increased coil resistance loss and increased weight. Since the specified currents are high and since core losses in ferrites are inherently low, the core size and numbers of turns were selected on the premise that the resistance loss in the coils would be the dominant loss. It was decided to use a small number of turns of heavy gauge wire, while satisfying the above minimum values for the N_p-core area products. Through an examination of the wide range of off-the-shelf toroids supplied by Magnetics Div. of Spang & Co., two sizes were identified that satisfied the above minimum values with reasonable N_p values. Key quantities defining these toroids are listed in Table 1.

Table 1. Selected Toroids and Numbers of Turns

	Transformer "a"	Transformer "b"
Magnetics Catalog No.	43825-TC	429154-TC
Material	J	J
D_o (mm)	38.1	29
D_i (mm)	19.05	19
h (mm)	25.4	15.2
βA_{core} (cm^2)	1.60	0.594
N_p	12	10
N_s	8	5
B_{max} (tesla)	0.228	0.245
Core Weight (g)	103.4	27.6
V_{core} (cm^3)	19.2	5.42

Although this selection does not reflect a rigorous optimization process, it probably represents the best combination of low loss and low weight that is attainable with off-the-shelf ferrite toroids. As this inverter concept advances toward flight hardware, it might be possible to gain significant weight reduction by using tape wound toroids of high performance magnetic alloys. These would accommodate a higher B_{max} which would allow smaller toroids to be used.

The coils are wound from stranded AWG-10 hook-up wire (37 strands of AWG-26 wire) with teflon insulation. The wire outer diameter is 3.4 mm and the resistance is 3.64 mΩ/m. Since the number of turns is small, each coil is wrapped tightly around the core in a single layer. The primary coil is wrapped directly around the core and the secondary coil is wrapped around the outside of the primary coil. Calculated coil lengths and resulting resistances are as follows. The lengths include a 6 inch leader at each end of each coil:

"a" Transformer - Primary

$$R_{pa} = 1.31 \text{ m} \times 3.64 = 4.77 \text{ m}\Omega$$

"a" Transformer - Secondary

$$R_{sa} = 1.19 \text{ m} \times 3.64 = 4.33 \text{ m}\Omega$$

"b" Transformer - Primary

$$R_{pb} = 0.844 \text{ m} \times 3.64 = 3.07 \text{ m}\Omega$$

"b" Transformer - Secondary

$$R_{sb} = 0.710 \text{ m} \times 3.64 = 2.58 \text{ m}\Omega$$

The i^2R loss in each coil can be calculated from the current amplitudes determined Section 2.2:

"a" Transformer - Primary

$$W_{pa} = R_{pa}\, i_{a0}^2 / 2 = 0.00477 \times 7.13^2 \div 2 = 0.121 \text{ watt}$$

"a" Transformer - Secondary

$$W_{sa} = R_{sa}\, i_{m0}^2 / 2 = 0.00433 \times 10.7^2 \div 2 = 0.248 \text{ watt}$$

"b" Transformer - Primary

$$W_{pb} = R_{pb}\, i_{b0}^2 / 2 = 0.00307 \times 5.35^2 \div 2 = 0.044 \text{ watt}$$

"b" Transformer - Secondary

$$W_{sb} = R_{sb}\, i_{m0}^2 / 2 = 0.00258 \times 10.7^2 \div 2 = 0.148 \text{ watt}$$

Core loss density in mwatt/cm^3 is specified by Magnetics as

$$P_c = K_c\, f^m\, B^n$$

where f has units of kHz, B has units of kgauss and K_c, m, and n are constants for a particular material. This expression is easily integrated over the toroid volume for the 1/r dependence of B, resulting in this expression for the total core loss

$$W_{core} = \alpha\, V_{core}\, K_c\, f^m\, B_{max}^n \qquad (23)$$

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where V_{core} is the core volume, specified in Table 1, and

$$\alpha = \frac{2\ (D_i/D_0)^2\ [1\ -\ (D_i/D_0)^{n\ -\ 2}]}{(n-2)\ \ [1\ -\ (D_i/D_o)^2\ ]} \qquad (24)$$

For Type J material

$K_c = 0.16$
$m = 1.67$
$n = 2.532$

The resulting core losses are

"a" Transformer

$\alpha = 0.387$

$W_{core\ a} = 0.387 \times 19.2 \times 0.16 \times 8^{1.67} \times 2.28^{2.532} \times 10^{-3} = 0.309$ watt

"b" Transformer

$\alpha = 0.569$

$W_{core\ b} = 0.569 \times 5.42 \times 0.16 \times 8^{1.67} \times 2.45^{2.532} \times 10^{-3} = 0.154$ watt

Table 2 summarizes the losses.

Table 2. Transformer Losses for 175 watt Inverter Output

	"a" Transformer	"b" Transformer
Primary i^2R	0.121	0.044
Secondary i^2R	0.248	0.148
Core	0.309	0.154
Total	0.678	0.346

For the six transformers, the total loss is 3.07 watts, which is only 1.8 % of the 175 watt output. The dominant loss for the inverter will be the i^2R loss in the MOSFET's which is described in the next section. These transformer designs show excellent efficiency based on these calculations. On this project they have been highly effective in demonstrating the large power transfer capability of this inverter concept. The emphasis for the transformers in the upcoming flight hardware development efforts will be to reduce their size and weight, probably by switching from ferrite to a tape wound magnetic alloy. This option should be explored at the earliest opportunity.

2.4 Switching Circuit

In this section, the MOSFET switches and associated electronics that generate the primary coil voltage waveforms will be described. Referring to Figures 1 and 2, the switching consists of the 6 MOSFET half-bridges with their IR2110 drivers, and the clock and D-type flip flop elements that generate the logic Q and Q signals to trigger the IR2110 drivers. The complete switching circuit is very compact physically, consisting of the MOSFET's, six IR2110 chips, two D flip-flop chips and one timing chip for the clock.

The breadboard inverter uses International Rectifier IRF540 N-channel power MOSFET's for the primary switches. The IRF540 was selected for its high continuous current capacity, fast switching time and relatively low on-state resistance (R_{ds}). Drain-to source breakdown voltage is 100 volt, safely above the specified 28 volt value of V_0. Continuous rated current is 28 amp at 25° C, safely above the specified 6.43 amp value of i_{p0}. Switching times, measured under actual operation of the breadboard inverter, are approximately 50 nanoseconds, resulting in negligible commutation loss. For the V_p switching pattern described in Section 2.1, there is no diode conduction in the reverse direction, except possibly at the instant of switching, because either the high side or the low side MOSFET of each half bridge is turned on at all times. This was not the case with the Phase I rotating field inverter or with preliminary versions of the present six transformer inverter. The avoidance of reverse conduction removes a significant source of switching loss.

The major MOSFET loss is that due to R_{ds}. For the IRF540 the maximum specified R_{ds} is 0.077 ohm. For each MOSFET, considering the 50% duty cycle of V_p, this loss is

$$W_{rds} = i_{p0}^2 R_{ds} / 4 = 6.43^2 \times 0.077 \div 4 = 0.796 \text{ watt}$$

For 12 MOSFET's this would total 9.55 watts, which is 5.5% of the 175 watt output. In the breadboard inverter, each switch consists of two MOSFET's connected in parallel. This effectively decreases R_{ds} by a factor of two, decreasing the total MOSFET loss to 4.78 watts, which is 2.7% of the 175 watt output. As well as reducing the loss, the use of two MOSFET's in parallel decreases the peak current carried by any one MOSFET to 3.2 amp at the 175 watt inverter output, which is only 11% of the 28 amp rating. This is a comfortable margin of safety for the MOSFET's.

The IR2110 bridge driver, also manufactured by International Rectifier, has provided a convenient solution to the normally difficult problem of driving an N-channel MOSFET on the high side of a half bridge. In the Phase I rotating field inverter and in the preliminary versions of the present inverter, this difficulty was overcome by using a P-channel MOSFET on the high side. The disadvantage of that approach is the high R_{ds} values characteristic of P-channel MOSFET's. For the IRF9540 P-channel MOSFET, which complements the IRF540 and was used in the earlier switching circuits, R_{ds} is 0.2 ohm, almost 3 times the R_{ds} of the IRF540. Since R_{ds} dominates the inverter losses, the advantage of using N-channel MOSFET's is obvious.

Figure 14 shows a schematic of the V_{p1} half bridge with the IR2110. The other five half bridges in Figure 1 are identical to this one. The gates of the two MOSFET's, are driven from the IR2110 outputs HO and LO which follow the logic signals at HIN and QIN. Driving the gate of the low side MOSFET (S2) is straightforward since the source is at ground. On the high side (S1) the source floats at V_{p1} so the IR2110 needs a floating supply voltage to switch to the gate. This is provided by the bootstrap capacitor C_b. When HO is low C_b is being

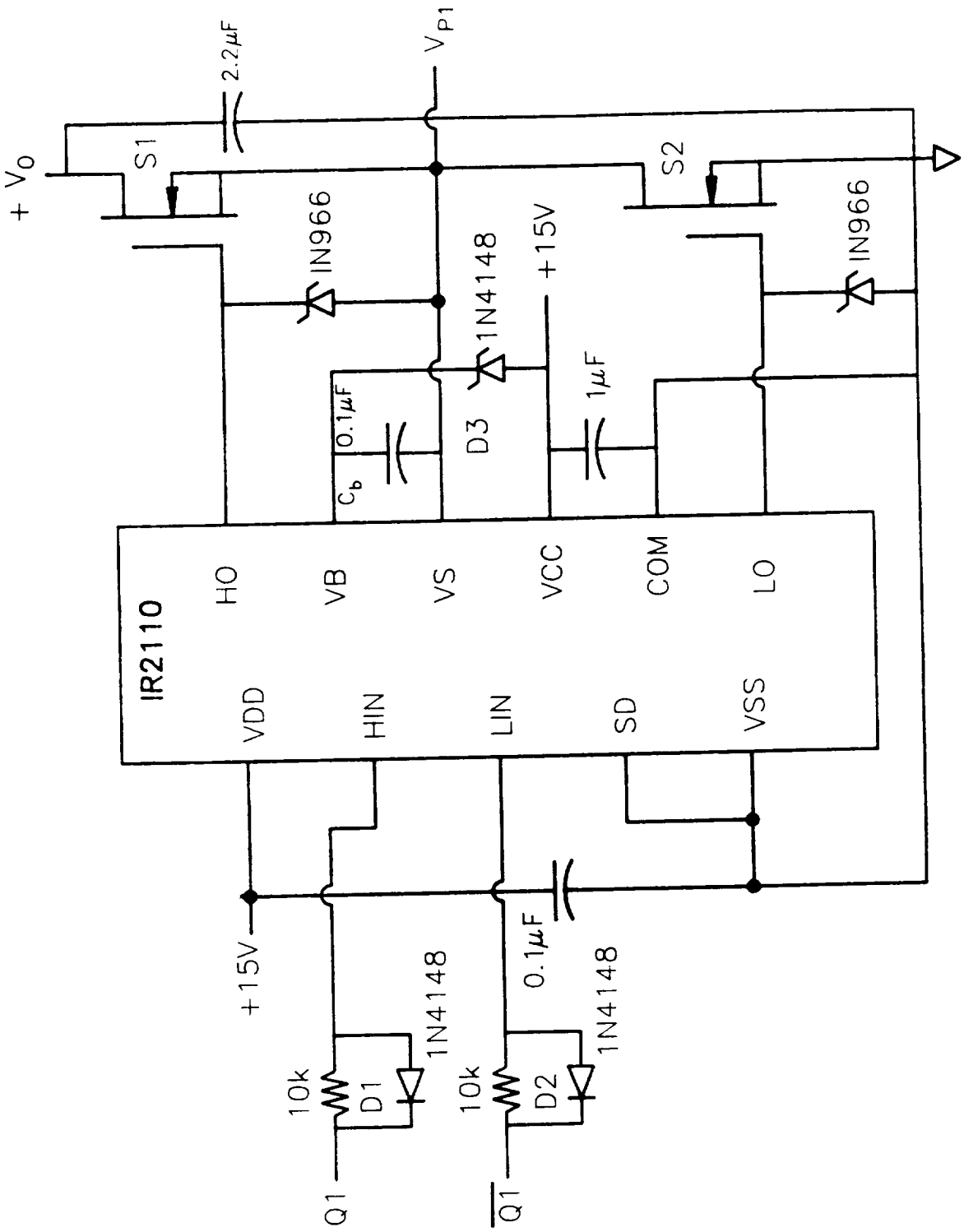

Figure 14. MOSFET HALF-BRIDGE WITH IR2110 DRIVER

charged through diode D3 from the 15 volt logic power supply. When HO is switched high, the voltage across C_b is transferred from VB to HO. C_b is sized to supply the required gate charge and to maintain the required gate-to-source voltage during the on time of S1. For the 4 to 8 kHz frequency range of the inverter, 0.1 μfarad has proven an adequate value for C_b. The required C_b can become prohibitively large in low frequency applications, necessitating the use of a floating DC power supply between VB and VS.

Switching of S1 and S2 occurs nominally at the same instant. The falling edge of the Q1 pulse that turns S1 off is coincident with the rising edge of the Q1 pulse that turns S2 on and vice versa. As mentioned above, this mode of simultaneously switching the high and low MOSFET's avoids losses associated with body diode conduction, which occurs when the two MOSFET's are off at the same time for some portion of the cycle. The risk in simultaneous switching is short circuit current between V_0 and ground at the instant of switching, occurring if one MOSFET turns on slightly before the other one turns off. The resistor-diode networks at HIN and LIN avoid this occurrence by delaying the the rising pulse edge that turns one MOSFET on relative to the falling pulse edge that turns the other one off.

Figure 15 shows the oscillator circuit that provides the clock signal for generation of the Q and $\bar{Q}$ signals by the D flip flops (Figures 1 and 2). The 555 timing chip, supplied with 15 volt DC, runs freely as a multivibrator, generating pulses of 50% duty cycle at the frequency

$$f_c = 1.44 / (R_c\, C_c)$$

The potentiometer for R_c provides a convenient means of setting f_c which is 12 times the inverter frequency. Over the full potentiometer range, f_c ranges over approximately 24 to 120 kHz, corresponding to inverter frequencies of 2 to 10 kHz.

2.5 Overall Performance and Efficiency

In the previous two sections transformer and MOSFET losses were calculated at the 175 watt specified design point for W_m. These are as follows:

Total Transformer Core Loss	1.39 watt
Total Transformer i^2R Loss	1.68 watt
Total MOSFET i^2R Loss	4.78 watt
Total Inverter Loss (W_{inv})	7.85 watt

Efficiency of the inverter is

$$\eta_{inv} = W_m / W_0 = W_m /(W_m + W_{inv}) = 175 \div (175 + 7.85) = 0.957$$

The effect of off-design operation on efficiency will now be analyzed. Since currents in the transformers and MOSFET's are proportional to i_{m0}, the total i^2R loss for the inverter is proportional to i_{m0}^2. For any value of i_{m0}, the total i^2R loss in watts, denoted by W_{res} can be expressed as

$$W_{res} = (1.68 + 4.78) \times (i_{m0} \div 10.7)^2 \;=\; 0.0565 \times i_{m0}^2 \qquad (25)$$

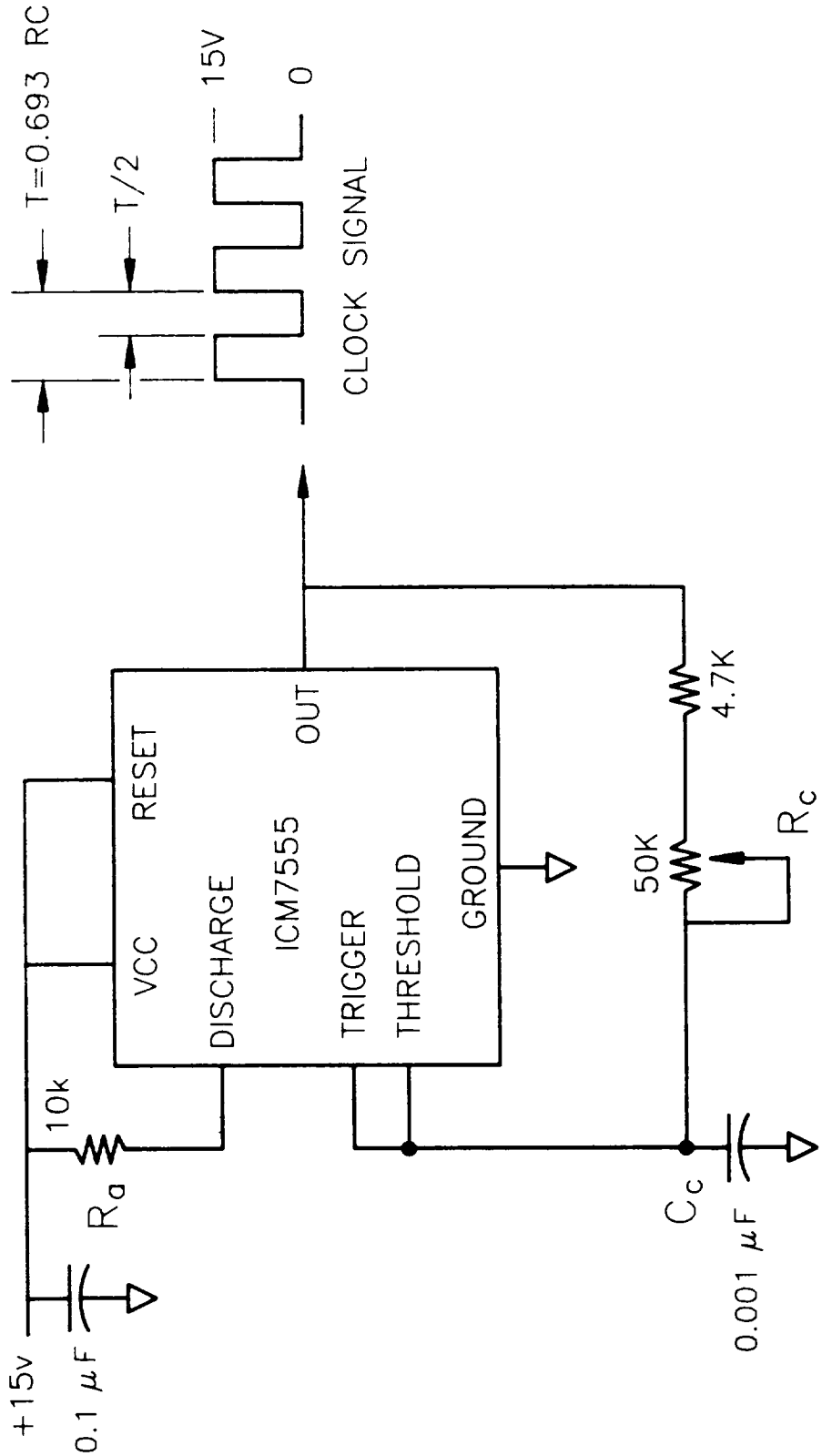

Figure 15. INTEGRATED CIRCUIT OSCILLATOR FOR CLOCK SIGNAL

where i_{m0} has units of amps.

A similar off-design relation can be derived for the core loss, which from Eq. (23) scales with

$$W_{core} \simeq f^m B_{max}^n$$

where m = 1.67 and n = 2.532.

for Magnetics Type J material. B_{max} scales with V_0/f, resulting in

$$W_{core} \simeq f^{m-n} V_0^n$$

Scaling from the design point values

$$W_{core} = 1.39 \times (f \div 8)^{-0.862} \times (V_0 \div 28)^{2.532} = 0.00181 \times f^{-0.862} \times V_0^{2.532} \quad (26)$$

where f is in kHz, V_0 is in volts and W_{core} is in watts. The total inverter loss, denoted by W_{inv} is then calculated as

$$W_{inv} = W_{res} + W_{core}$$

Finally, W_m is calculated from

$$W_m = (3/2)\, i_{m0}\, V_{m0} \cos\theta$$

where V_{m0} is proportional to V_0.

Inverter efficiency can be written in the form

$$1 / \eta_{inv} = 1 + W_{inv} / W_m$$

If core loss is ignored, a reasonable approximation for the present design, the above equations for W_{res} and W_m can be substituted to give the approximate expression

$$1 / \eta_{inv} = 1 + 0.0251\, W_m / (V_{m0} \cos\theta)^2$$

which to first order is equivalent to

$$\eta_{inv} = 1 - 0.0251\, W_m / (V_{m0} \cos\theta)^2$$

This shows the impact of off-design operation on efficiency of the inverter. At the design point, this equation gives

$$\eta_{inv} = 1 - 0.0251 \times 175 \div (21.8 \times 0.5)^2 = 1 - 0.0370 = 0.963$$

If W_m is increased by a factor of 2 at the same $V_{m0} \cos\theta$ the efficiency decreases to

$$\eta_{inv} = 1 - 2 \times 0.0370 = 0.926$$

representing a 4 point decrease. If $V_{m0} \cos\theta$ is decreased by a factor of 2 at the design W_m, the efficiency decreases more dramatically to

$$\eta_{inv} = 1 - 0.0370 \times 4 = 0.852$$

representing an 11 point decrease. This illustrates the importance of matching the inverter design to the characteristics of the motor. Off design operation of the motor at either reduced voltage or reduced power factor has a strong negative impact on inverter efficiency. This comes into play at reduced frequency. Since the magnetic field in both the motor and the inverter is proportional to V_{m0}/f, V_{m0} may have to be reduced to avoid saturation if f is reduced. Saturation resulting from a failure to reduce V_{m0} would carry the penalty of an even more severe reduction in cos θ, which would be the manifestation of a sharp increase in i_{m0}. These trends are discussed further in Section 3.2.3.

2.6 Packaging of Breadboard Inverter

The breadboard inverter, shown by photographs in Figures 16 and 17, consists of a perforated wire wrap board containing all of the electronic components, including the MOSFET's and drivers, with the six toroidal transformers clustered beneath the board. The board is hexagonal in shape, with a diagonal extent of 7.25 inch. Logic components are wire wrapped but the MOSFET and transformer terminals are soldered. To minimize noise which takes the form of spikes at the V_p pulse edges, care was taken to make the leads between the MOSFET's and the V_0 and ground rails as short as possible. This makes the lead inductance as low as possible.

Each of the twelve switches, consisting of two paralleled MOSFET's was constructed as a module with a through bolt connecting the MOSFET cases to a small aluminum spacer block and a pair of heat sinks. The six high side and low side switch pairs occupy the vertices of the hexagonal board as shown by Figure 16. The V_0 and ground power rails run along the periphery of the board on the underside, straddled by the MOSFET leads so as to minimize the length of those leads. The rails consist of lengths of AWG-10 hook-up wire, appear in Figure 16 as short jumpers around the board vertices, connecting the output terminal of each pair of switches to the ring of primary coils on the underside. The remaining electronics, consisting of the IR2110 bridge drivers, two D-type flip-flop chips, the 555 timing chip, and their associated discrete components, occupy the interior of the hexagon. The six 2.2 μfarad filter capacitors, one for each pair of MOSFET switches are soldered between the two rails on the underside. An additional filter capacitor is placed across the rail terminals.

The preliminary design of the engineering model inverter, which is described in Section 4, uses the same general architecture of the breadboard, with the above arrangement of components incorporated on a single PC board.

The aluminum plate, to which the inverter assembly is mounted, is the base of a freon calorimeter vessel which was used to verify the inverter loss calculations of the preceding sections. Figure 17 shows this base plate. Figure 18 shows the cylindrical vessel which fits over the inverter and bolts to the base plate. Inside the vessel the inverter is immersed in liquid freon. Urethane foam insulation, approximately 4 inches thick, surrounds the vessel on all surfaces. When the inverter is operating at steady state, the boil off rate of the liquid freon provides a measure of the total inverter loss. Operating procedures and results with the calorimeter are described in Section 3.

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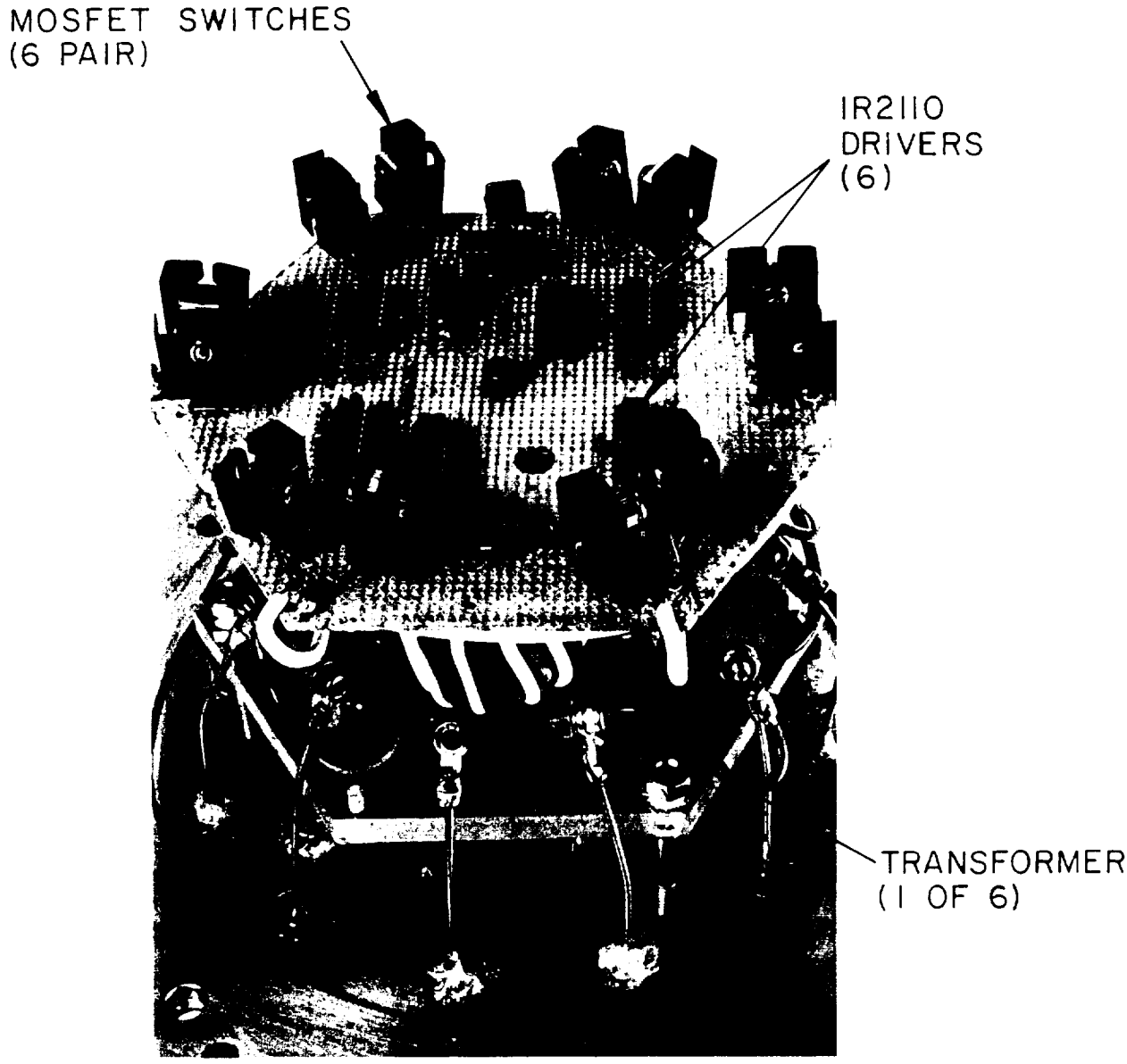

Figure 16. BREADBOARD INVERTER - TOP VIEW

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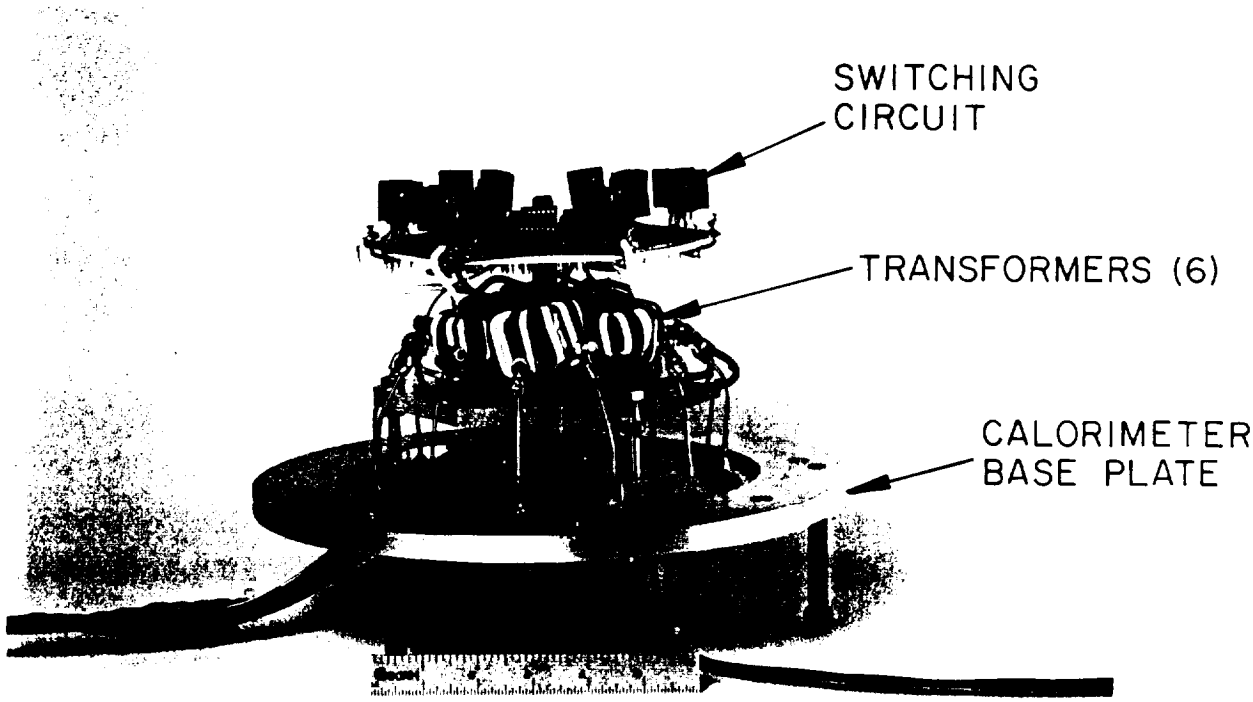

Figure 17. BREADBOARD INVERTER - SIDE VIEW

BLACK AND WHITE PHOTOGRAPH

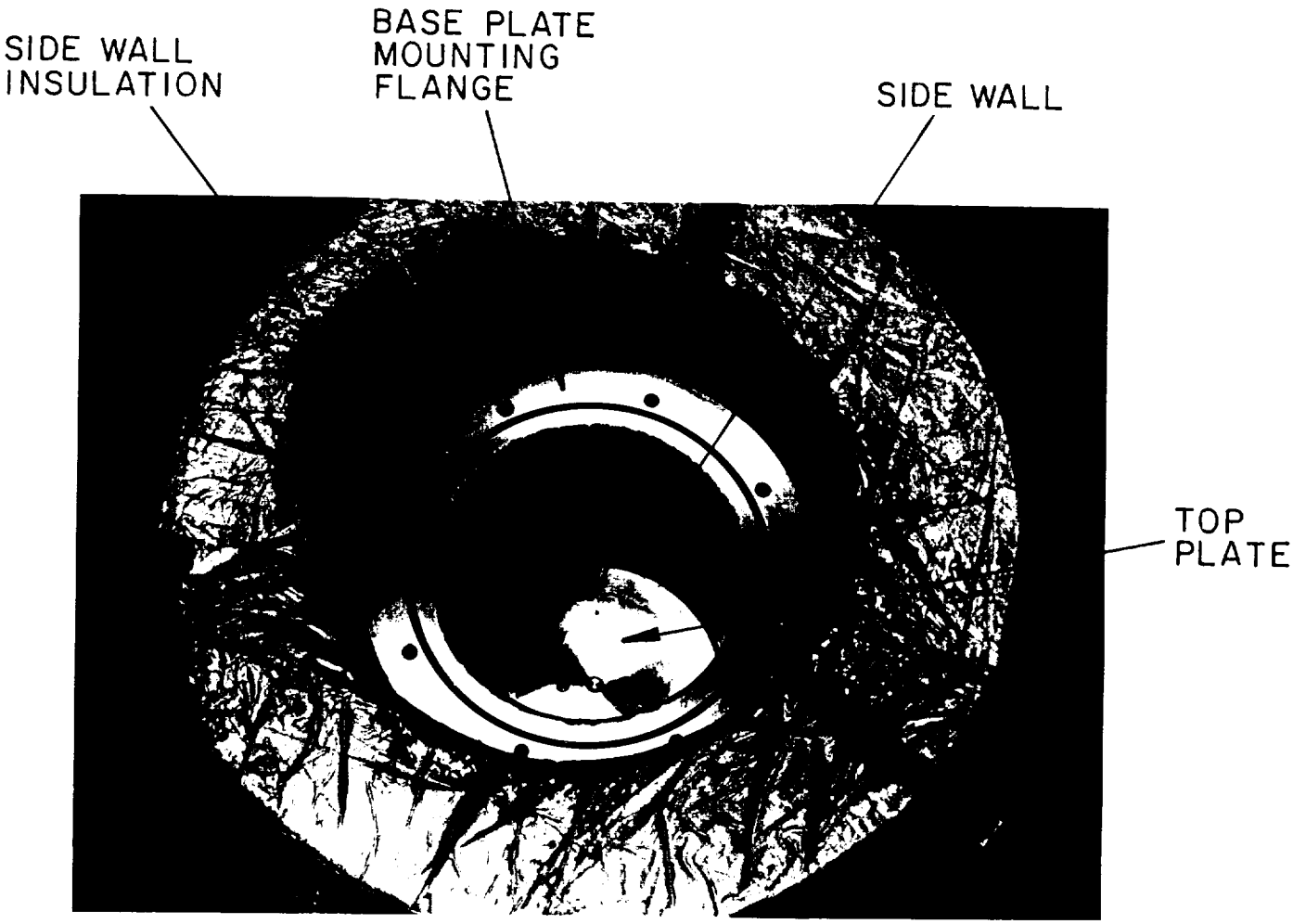

Figure 18. BREADBOARD INVERTER - CALORIMETER VESSEL
(VIEW FROM BOTTOM WITH INVERTER
AND BASE PLATE REMOVED)

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2.7 Inverter Controls

Based on the foregoing descriptions of inverter operation, there are only two controllable variables that can influence the output voltage waveform. These are the DC input voltage V_0, which governs the output amplitude V_{m0} according to

$$V_{m0} = (2/3)\,[(N_{sa}/N_{pa}) + (N_{sb}/N_{pb})]\,V_0$$

and the clock frequency f_c which governs the output frequency f according to

$$f = f_c / 12$$

Given that V_0 is maintained by the DC power source, the current waveforms are governed by the output impedance which depends on the motor's load and operating characteristics.

Strategy for control of the inverter is dictated by the anticipated modes of operation of the SSRB cryocooler. At this point only a single operating speed is envisioned for the compressor, corresponding approximately to the specified 8 kHz frequency of the breadboard inverter. In the breadboard the frequency can be varied by varying the potentiometer setting that determines R_c in the clock circuit. In a future flight version, a fixed trim pot would fix R_c for normal operation. For starting, a logic command to the clock circuit would switch a higher resistance value into the R_c network to provide a lower frequency on the order of 4 kHz. After allowing sufficient time for the compressor to reach 4 kHz, a second logic command would switch the normal resistance value into the R_c network.

With the inverter frequency fixed, the compressor's rotational speed is governed by the voltage amplitude V_{m0} applied to the induction motor. The mechanism for this is described in Section 3.2.3. From a control standpoint, variation in V_{m0} is undesirable because the accompanying variation in rotational speed would change the thermodynamic operating condition of the compressor. Based on the breadboard compressor tests (Section 3.2.3), the maximum tolerable variation in V_{m0} is typically ±2%. Since V_{m0} is proportional to V_0, the tolerance on V_0 is ±2%.

In testing the breadboard inverter and compressor, DC power was provided by a Sorenson Model DCR 40-25B power supply. This is a high quality commercial DC supply for laboratory or industrial use which allows V_0 to be set manually and holds the setting within a regulation of 0.05%. In a spaceflight application, the inverter is nominally required to accept power from an unregulated DC bus whose voltage can vary over 28 ± 6 volts. A pre-regulator would be needed to supply DC voltage to the inverter within a ±2% tolerance. Fairchild Space performed a preliminary survey of pre-regulator designs for this application and concluded that a boost mode DC-to-DC converter with no transformer isolation would be suitable. (Transformer isolation of the motor from the bus is provided by the inverter itself.)

Figure 19 shows a schematic of the electrical power system for the SSRB cryocooler incorporating a pre-regulator with an unconditioned 28 volt bus. Although V_0, which is the output voltage of the pre-regulator, was specified as 28 volts for the breadboard inverter design, it is left unspecified in this schematic. There will be a power loss in the pre-regulator and V_0 should be selected so as to minimize the combined loss of the inverter and pre-regulator. The inverter design concept allows a wide latitude for the selection of V_0. For a given ratio V_{m0}/V_0, the transformer turns ratios are simply selected according to Eqs. (21) and (22). For the same power, for example, an inverter designed for V_0 = 56 volts, as opposed

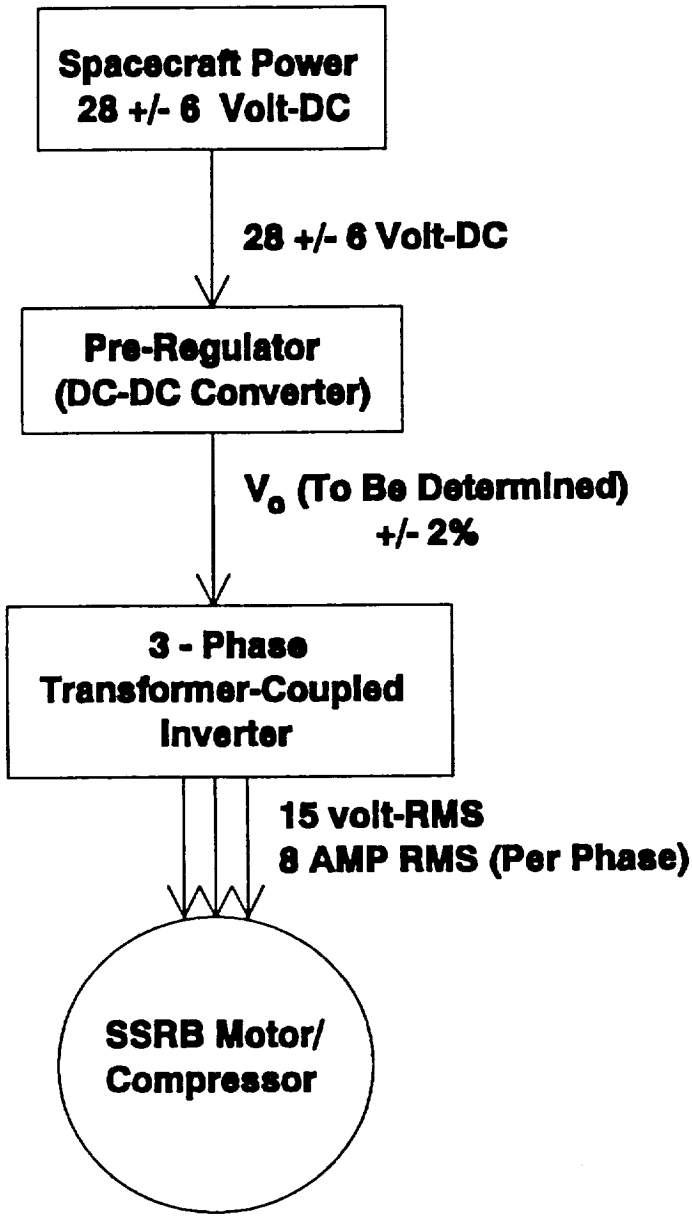


Figure 19. SCHEMATIC OF SSRB POWER SYSTEM WITH PRE-REGULATOR

to 28 volts, would have one-half the primary lead current amplitude i_{p0}. MOSFET loss would be reduced by a factor of 4, offsetting some of the pre-regulator loss.

In power systems envisioned for future scientific space platforms, regulated DC power at 100 to 120 volts would be available, possibly making a pre-regulator unnecessary. An inverter designed for this DC input level would be highly efficient. At V_0 = 112 volts, for instance, i_{p0} would decrease by a factor of 4 relative to 28 volts. The consequent decrease in MOSFET loss would be diminished slightly because MOSFET's with a higher voltage rating, which have a higher value of R_{ds}, would be needed. A suitable MOSFET, of the same class used in the breadboard, is the International Rectifier IRF640. The drain-to-source breakdown voltage for the IRF640 is 200 volts, and the maximum R_{ds} is 0.18 Ω, compared with 100 volts and 0.077 Ω for the IRF540 used in the breadboard. For the IRF640 with V_0 = 112 volts, MOSFET loss relative to the breadboard inverter would decrease by the factor

$$0.18 \div 0.077 \div 4^2 = 0.146$$

Operation at higher values of V_0 is clearly beneficial for the inverter. Transformer losses do not change significantly with V_0, but, as just shown, MOSFET losses decrease substantially. Limitations on V_0 would be associated with losses in the pre-regulator, if one is needed.

The envisioned starting procedure for a flight unit, based on the start-up test results that are described in Section 3.2.4, is to switch the inverter on at a reduced voltage and frequency, wait a prescribed period of time to allow the compressor to accelerate from zero speed to this starting frequency, then switch to the design voltage and frequency. This procedure is completely open loop. The sequence of events will be executed by simple logic elements incorporated in the inverter switching circuit. The only external communication to the inverter circuit would be a logic command to start or stop the inverter. The reduced starting voltage will be provided by a series resistance between the pre-regulator and inverter that is bypassed during normal operation.

No significant variation in the electrical load from the compressor motor is expected during normal operation. DC current drawn by the inverter will therefore be steady. Overcurrent protection of some form will be provided to protect the inverter and motor from unanticipated failure modes of the compressor.

It should be emphasized that the induction motor and inverter constitute a conventional open loop drive system. The control philosophy is to utilize this fact to the fullest in developing a system that is simple and robust with excellent potential for long term reliability.

3. BREADBOARD INVERTER TESTS

3.1 Performance with Dummy Load

A standard dummy load, consisting of a parallel resistance and reactance for each phase, was used throughout the project to evaluate the inverter at its various stages of development. Figure 8 shows the configuration of this load, which simulates the specified 175 watt motor load at $V_0 = 28$ volt and $\theta = 60°$. The load resistances have the value $R = 4\ \Omega$. Each resistance consists of a bank of eight 2 Ω power resistors mounted to a large heat sink. Each load reactance consists of a 44.5 μh inductance, obtained from approximately 85 turns of stranded AWG-16 wire wound on a hollow plastic cylinder of 1-inch OD by 7.5-inch length. For f = 8 kHz, the actual reactance and power factor angle are

$$X = 2\pi \times 8000 \times 44.5 \times 10^{-6} = 2.24\ \Omega$$

$$\theta = \mathrm{Tan}^{-1}\ (4 \div 2.24) = 60.8°$$

The measured resistance value for each inductor is

$$R_x = 0.143\ \Omega$$

For tests with the dummy load, input power at $V_0 = 28$ volt was provided by the Sorenson power supply and the clock potentiometer was set for f = 8 kHz. Voltage and current waveforms were recorded with a Hewlett Packard 54501A Digitizing Oscilloscope, and a Tektronix A6303 and AM503 current probe and amplifier. Input voltage (V_0) was measured with a Hewlett Packard 3478A digital voltmeter. This measurement is taken across the power rail terminals on the inverter circuit board so as to avoid any voltage drop along the power supply leads. Input current (i_0) was obtained by using a second digital voltmeter of the same model to measure the voltage drop across a precision 10 mΩ shunt resistor placed in series with one of the power supply leads. 15 volt biasing for the logic components was provided by a Heath 2718 DC supply.

The measured DC input current for the dummy load test is

$$i_0 = 6.83\ \mathrm{amp}$$

resulting in an input power of

$$W_0 = 28 \times 6.83 = 191\ \mathrm{watt}$$

A complete set of waveforms consisting of V_m, V_p, i_r, i_x, i_m and i_p is shown in Figures 20-24 for the three phases. In all cases, waveshapes can be seen to correspond closely to the calculated waveshapes described in Section 2.1. The predicted saw tooth irregularities in the i_m and i_p waveshapes are clearly exhibited by the measured waveshapes. Waveshape amplitudes agree well with values predicted from the Equations (14)-(18).

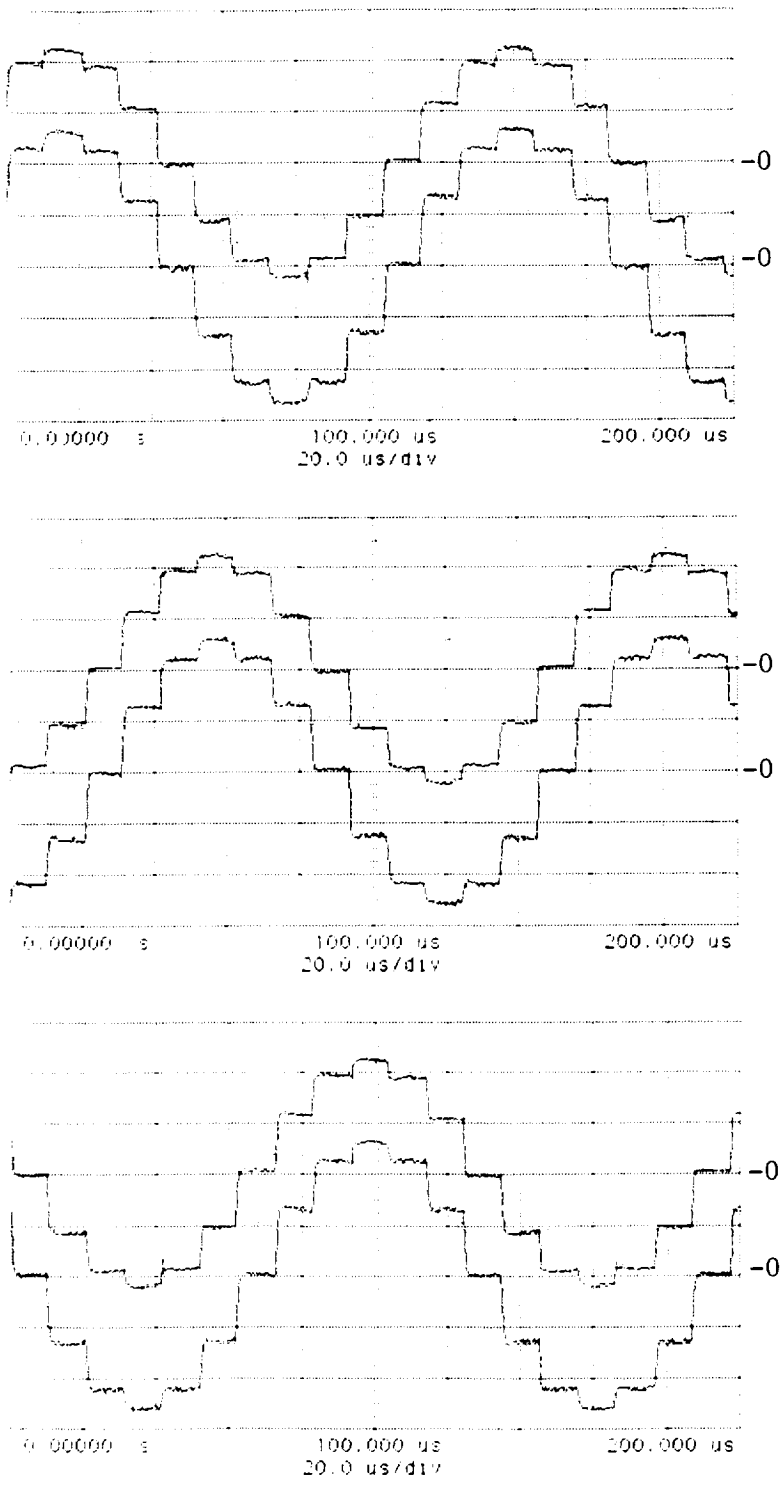
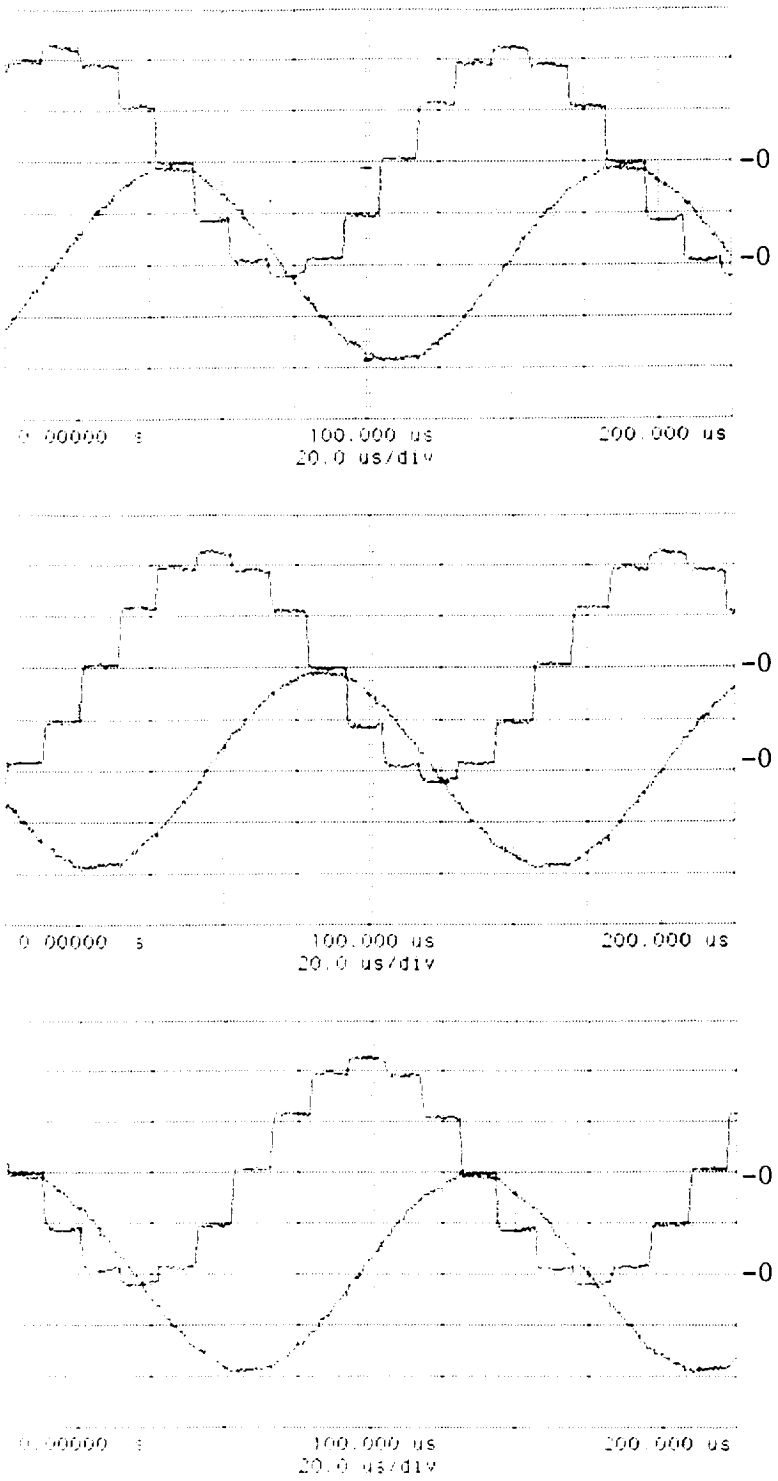


Figure 20. MEASURED LOAD VOLTAGE AND RESISTIVE CURRENT WAVEFORMS FOR BREADBOARD INVERTER WITH DUMMY LOAD: f = 8 KHZ; V_o = 28 volt; i_o = 6.83 amp



V_{m1} (10.0 volt/div)

i_{x1} (5.0 amp/div)

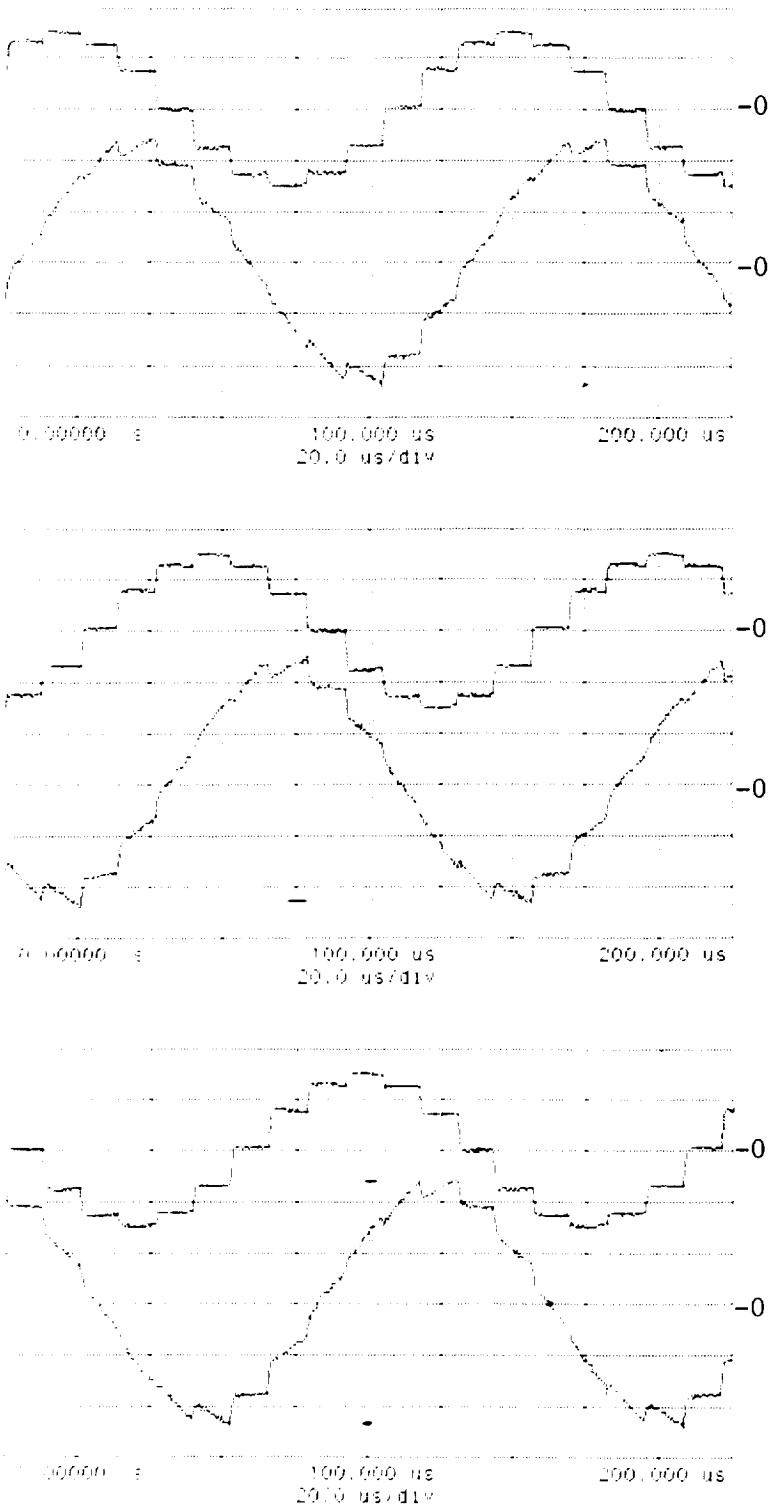
V_{m2} (10.0 volt/div)

i_{x2} (5.0 amp/div)

V_{m3} (10.0 volt/div)

i_{x3} (5.0 amp/div)

Figure 21. MEASURED LOAD VOLTAGE AND REACTIVE CURRENT WAVEFORMS FOR BREADBOARD INVERTER WITH DUMMY LOAD: f = 8 kHz; V_o - 28 VOLT; i_o = 6.83 AMP



V_{m1} (15.0 volt/div)

i_{m1} (5.0 amp/div)

V_{m2} (15.0 volt/div)

i_{m2} (5.0 amp/div)

V_{m3} (15.0 volt/div)

i_{m3} (5.0 amp/div)

Figure 22. MEASURED LOAD VOLTAGE AND TOTAL CURRENT WAVEFORMS FOR BREADBOARD INVERTER WITH DUMMY LOAD: f = 8 kHz; V_o = 28 VOLT; i_o = 6.83 AMP

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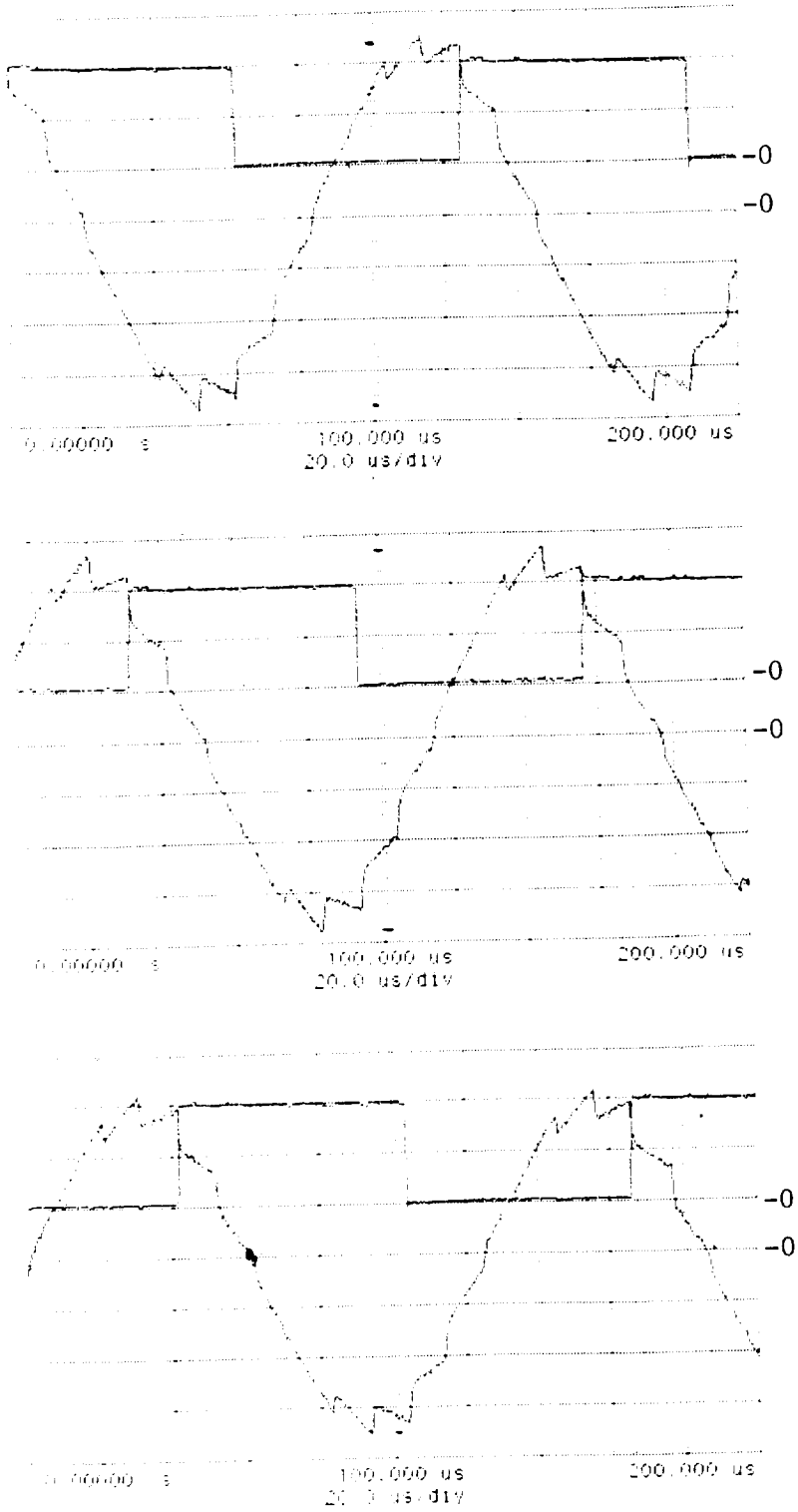


V_{p1} (15.0 volt/div)

i_{p1} (2.0 amp/div)

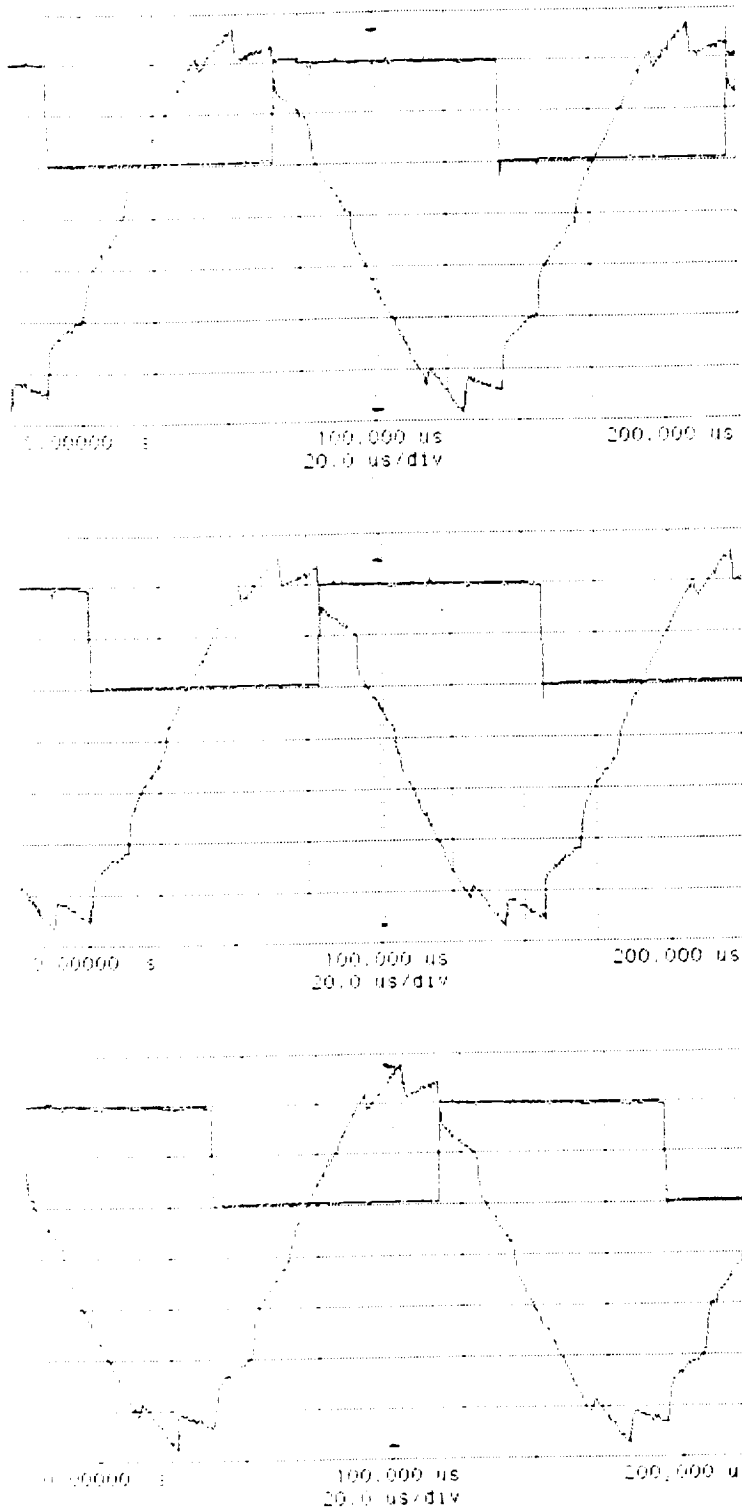
V_{p2} (15.0 volt/div)

i_{p2} (2.0 amp/div)

V_{p3} (15.0 volt/div)

i_{p3} (2.0 amp/div)

Figure 23. MEASURED VOLTAGE AND CURRENT WAVEFORMS AT PRIMARY LEADS 1 - 3 FOR BREADBOARD INVERTER WITH DUMMY LOAD: f = 8 kHz; V_o = 28 VOLT; i_o = 6.83 AMP



V_{p4} (15.0 volt/div)

i_{p4} (2.0 amp/div)

V_{p5} (15.0 volt/div)

i_{p5} (2.0 amp/div)

V_{p6} (15.0 volt/div)

i_{p6} (2.0 amp/div)

Figure 24. VOLTAGE AND CURRENT WAVEFORMS AT PRIMARY LEADS 4 - 6 FOR BREADBOARD INVERTER WITH DUMMY LOAD: f = 8 kHz; V_o = 28 VOLT; i_o = 6.83 AMP

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For the test parameters

$N_{sa}/N_{pa} = 2/3$ $\quad N_{sb}/N_{pb} = 1/2$
$R = 4\ \Omega$ $\quad \theta = 60.8°$ $\quad V_o = 28$ volt

Equations (14) - (18) predict

$V_{m0} = (2/3) \times (2/3 + 1/2) \times 28 = 21.8$ volt
$i_{m0} = 21.8 + (4 \times \cos 60.8°) = 11.2$ amp
$i_{a0} = (2/3) \times 11.2 = 7.47$ amp
$i_{b0} = (1/2) \times 11.2 = 5.60$ amp
$i_{p0} = [7.47^2 + 5.60^2 - 7.47 \times 5.60]^{\frac{1}{2}} = 6.73$ amp

while the measured waveforms show

$V_{m0} = 22$ to 23 volt
$i_{m0} = 11$ to 12 amp
$i_{p0} = 6$ to 7 amp

Predicted inverter losses for this test can be obtained from Eqs. (25) and (26) for W_{res} and W_{core}:

$$W_{res} = 0.0565 \times 11.2^2 = 7.09 \text{ watt}$$

$$W_{core} = 0.00181 \times 8^{-0.862} \times 28^{2.532} = 1.39 \text{ watt}$$

$$W_{inv} = 7.09 + 1.39 = 8.48 \text{ watt}$$

This total loss is too small a value to be resolved by subtracting the calculated output power from the calculated input power. Consider the following estimate of output power for $i_{m0} = 11.2$ amp:

Load Resistors	$3 \times 4\ \Omega \times (11.2 \times \cos 60.8°)^2 \div 2$ = 179 watt
Load Inductors	$3 \times 0.143\ \Omega \times (11.2 \times \sin 60.8°)^2 \div 2$ = 20 watt
Total	$W_m = 179 + 20 = 199$ watt

The apparent 8 watt gain over $W_0 = 191$ watt as opposed to an expected 8.5 watt loss reflects the uncertainty associated with the extraction of equivalent sine wave amplitudes from the real non-sinusoidal waveforms.

The freon calorimeter described in the next section was developed as a more certain means to verify the direct prediction of inverter losses given in Section 2.5. Based on the above direct calculations of W_0 and W_{inv} the predicted inverter efficiency for the dummy load test is

$$\eta_{inv} = (191 - 8.5) \div 191 = 0.955$$

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3.2 Compressor Tests

Tests of the SSRB compressor with the breadboard inverter were coordinated with the concurrent development project for the SSRB cryocooler (NASA Contract NAS5-31281). For the present inverter project the tests had two objectives. The first was to demonstrate the capability of the inverter to drive the compressor at its design speed and load. The second was to demonstrate that the inverter can supply the maximum starting current drawn by the compressor's induction motor. Both objectives were successfully met by the tests. The following four sub-sections give descriptions of the compressor test facility, the inverter calorimetry experiments, the measured steady-state performance of the compressor and inverter over a wide range of conditions, and the measured start-up performance. Further detail on the test facility, the compressor and bearing hardware, and the analysis of compressor and motor losses can be found in reports presently under preparation for Contract NAS5-31281.

3.2.1 Facility and Instrumentation

Figure 25 shows a schematic drawing of the compressor test facility, including the breadboard inverter and calorimeter. All inverter electrical measurements are as described Section 3.1 for the dummy load tests. Instruments VM1 and VM2 are the digital voltmeters that measure V_0 and i_0. Resistors RS and RP represent the precision shunt for i_0 and the frequency adjusting potentiometer for the clock circuit.

All information on performance of the compressor is obtained from measurement of inlet pressure and temperature (P1, T1), exit pressure (P2), mass flow (FM, P3, T3), and shaft speed (CP2). Instrument FM is a turbine flowmeter which measures the volumetric flow rate leaving the compressor. Measurement of P3 and T3 provides the density at the flowmeter needed to determine the mass flow. CP1 and CP2 are capacitance probes which monitor radial position and rotational speed of the compressor shaft. The thermocouple, pressure transducer and flowmeter data were recorded through a data acquisition system consisting of ASYST software and an IBM personal computer.

The tests were run in air with the compressor inlet open to the atmosphere. A particular operating condition is fixed by the inverter frequency f, inverter input voltage V_0 and the amount of opening of the throttle V1 in the compressor exit line.

The calorimeter operates on the principle that all energy dissipated within the inverter is absorbed through boiling of the liquid freon in which it is immersed. Boil-off vapor exits the calorimeter vessel into a water-cooled condenser. The condensed vapor fills a graduated burette. The rate at which liquid fills the burette, as timed with a stop watch, determines the total inverter loss. This measurement is described in detail in the following sub-section.

3.2.2 Calorimeter Results

The calorimeter working fluid is Freon-11, supplied by DuPont. Key thermal properties are listed in Table 3.

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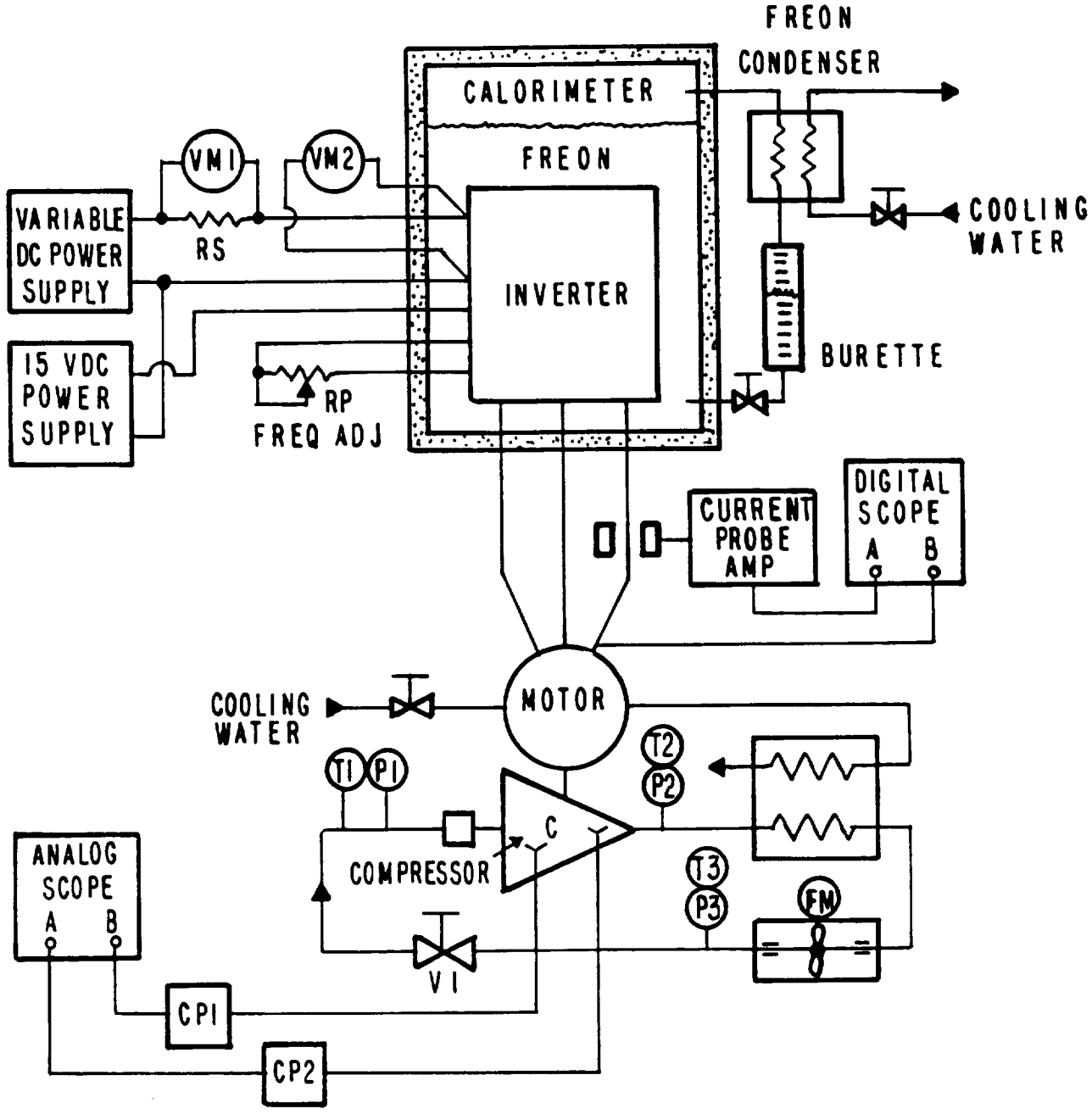

Figure 25. TEST FACILITY FOR SSRB COMPRESSOR WITH BREADBOARD INVERTER

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Table 3. Properties of Freon-11	
Boiling Point at 1.0 atm	T_{sat} = 23.82° C
Liquid Density at 25° C	ρ_f = 1.476 g/cc
Sat. Vapor Density at Boiling Point	ρ_v = 0.00586 g/cc
Heat of Vaporization at Boiling Point	h_{fg} = 180.3 joule/g
Liquid Heat Capacity at 25° C	c_{pf} = 0.871 joule/g-°C

Equating total inverter loss to the rate of energy absorbed by boiling gives the relation

$$W_{inv} = \rho_f Q_f h_{fg}$$

where Q_f is the boil-off flow rate of liquid. From the values in Table 3

$$Q_f \text{ [cc/s]} = W_{inv} \text{ [watt]} / (1.476 \times 180.3)$$
$$= W_{inv} \text{ [watt]} / 266$$

The burette, which captures the liquid boil-off, has a capacity of 50 cc and a height of approximately 54 cm. It is graduated in 0.1 cc increments, with approximately 1.08 mm between gradations. The operating procedure that evolved in shaking down the calorimeter apparatus was to record, using a stop watch, the time required for the liquid level to rise 10 gradations, or 1.0 cc. This time, denoted as t_{cc} is the inverse of Q_f. The corresponding inverter loss is then given by

$$W_{inv} \text{ [watt]} = 266 / t_{cc} \text{ [s]}$$

The objective in shaking down the calorimeter was to ensure satisfaction of this relation under a known power input representing the variable W_{inv}. A bank of electrical resistors, immersed in the freon tank and driven from a DC power supply, provided the known power input. If this could be achieved, the above equation could be used confidently in determining an unknown W_{inv} from a measured value of t_{cc}.

Successful operation of the calorimeter requires stable environmental conditions and low heat leak. These were achieved through thorough insulation of the vessel, the vapor exit line and the liquid return line. In using the calorimeter, the burette was kept approximately half filled at all times, cyclically letting the level rise for 5 to 10 cc as readings were taken and then dumping the 5 to 10 cc of liquid back into the vessel by opening a stop-cock at the bottom of the burette.

Despite the above efforts, the calorimeter still proved to be highly sensitive to small changes in environmental conditions, particularly changes in temperature of the room air or the condenser cooling water. Environmental changes would lead to condensation in the exit line or boiling in the return line, causing the measured burette fill rate to drift significantly. Significant progress was made in correcting these problems, but the project did not have the time or money to complete the effort. Enough valid data points were acquired to establish confidence in the inverter loss models derived in Section 2, but the danger of environmental drift and the need to allow significant time for readings to stabilize, precluded use of the calorimeter for direct measurement of the inverter loss at each compressor test point. Inverter losses were instead calculated from the measured motor current and voltage.

The most convincing calorimeter data point was acquired in a test where the compressor was run from the inverter immediately following a period of stable performance of the calorimeter with a known 10 watt input and four successive readings of t_{cc} ranging from 26.0 to 26.3 sec. The compressor was operated with the inverter set for V_0 = 15.6 volt and f = 5 kHz, and a moderate throttle opening. The input current at this condition was i_0 = 7.7 amp resulting in

$$W_0 = 15.6 \times 7.7 = 120 \text{ watt}$$

Figure 26 shows the motor voltage and current waveforms for the three phases from which

$$i_{m0} = 16 \text{ amp}$$

A succession of 10 burette readings ranged from 24.2 to 25.6 sec. Dividing these values into 266 gives a range of

$$W_{inv} = 10.4 \text{ to } 11.0 \text{ watt}$$

For comparison the losses can be calculated from Equations (11) and (12):

$$W_{res} = 0.0565 \times 16.0^2 = 14.46 \text{ watt}$$

$$W_{core} = 0.00181 \times 5^{-0.532} \times 15.6^{2.532} = 0.47 \text{ watt}$$

$$W_{inv} = 14.46 + 0.47 = 14.9 \text{ watt}$$

This predicted loss exceeds the calorimeter measurement by approximately 40%. Since the MOSFET's dominate the loss, and since the manufacturer's specified maximum value of R_{ds} (0.077 Ω) is being used to calculate the loss, a measurement of the actual R_{ds} value was made in situ to see if it could account for the discrepancy. This was done by separately supplying DC current from V_0 to ground through each pair of high and low MOSFET switches, and measuring the V_0 values for currents of 6, 8 and 10 amp. The switch pair being measured was turned on by supplying 15 volt DC to the gates. The other five switch pairs were off, making the switches being measured the only path from V_0 to ground. Since each switch is comprised of two MOSFET's in parallel, the effective combined resistance of the high and low switches is the average R_{ds} of the four MOSFET's. Based on the V_0 value at 10 amp, the measured R_{ds} value averaged over the six switch pairs is 0.046 ohm.

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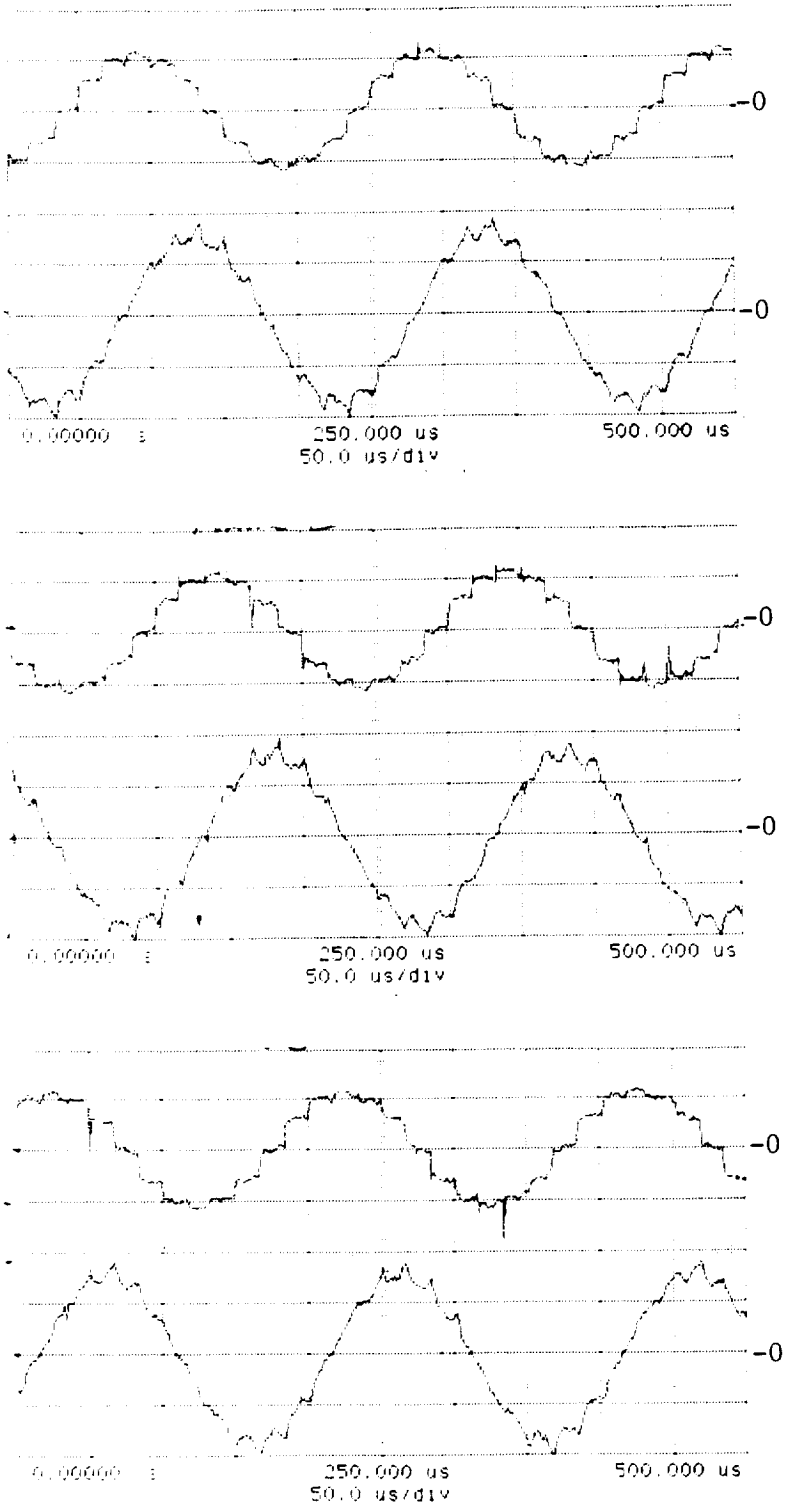

V_{m1} (10.0 volt/div)

i_{m1} (10.0 amp/div)

V_{m2} (10.0 volt/div)

i_{m2} (10.0 amp/div)

V_{m3} (10.0 volt/div)

i_{m3} (10.0 amp/div)

Figure 26. MEASURED MOTOR VOLTAGE AND TOTAL CURRENT WAVEFORMS FOR BREADBOARD INVERTER FROM TEST OF COMPRESSOR AND CALORIMETER: F = 5 kHz; V_o = 15.6 VOLT; i_o = 7.7 AMP

Using this measured R_{ds} value, previously calculated MOSFET losses should be reduced by a factor of 0.046 + 0.077 = 0.60. This should account for the 40% discrepancy. Equation (11) of Section 2.5 can be corrected as follows:

$$W_{res} = (1.68 + 4.78 \times 0.60) \times (i_{m0} + 10.7)^2 = 0.0397 \times i_{m0}^2 \quad (27)$$

The predicted inverter loss for this calorimeter data point now becomes

$$W_{inv} = W_{core} + W_{res} = 0.47 + 0.0397 \times 16.0^2 = 10.6 \text{ watt}$$

This shows perfect agreement with the calorimeter measurement. On the basis of this agreement, Equation (12) for W_{core} and Equation (13) for W_{res} are used to calculate the inverter loss from the measured values of i_{m0}, V_{m0} and f in the compressor tests described in the following sub-section.

3.2.3 Steady-State Performance Tests

Performance data were obtained at inverter frequencies of 5, 6, 7, 8, and 9 kHz over a range of throttle openings. For each combination of inverter frequency and throttle opening, readings were taken at three voltages to determine how slip of the induction motor influences performance of the motor and inverter. Shaft speed (f_s) and throttle opening fix the operating point of the compressor, which is represented by pressure ratio (PR), and mass flow (m). The relation between shaft speed and inverter frequency is represented by the slip parameter (s), defined as

$$s = (f - f_s) / f$$

In conducting the tests, f and the throttle opening were fixed. As the motor voltage V_{m0} was varied, f_s varied within a small range slightly lower than f ($s \leq 0.1$). This variation in V_{m0} and s had a weak influence on the compressor operating point through the small changes in f_s, but a stronger influence on the motor and inverter losses.

Tables in Appendix A contain spreadsheet listings of the test data, grouped according to the five frequencies. There are two tables for each frequency, the first containing directly measured quantities and the second containing performance variables calculated from the directly measured quantities. Blank rows separate the groups of tests points taken at a fixed throttle opening. The last three tables define the symbols used for the spreadsheet column headings and list the constants and equations for the performance calculations. The inverter loss calculation uses Equations (12) and (13) as discussed in Section 3.2.2.

The matrix of test points covers a shaft speed (f_s) range of 4400 to 8600 rev/s, a mass flow (m) range of 0.3 to 1.7 g/s and a pressure ratio (PR) range of 1.1 to 2.2. The isentropic enthalpy rise for the compressor at some inlet temperature T_1 and pressure ratio is given by

$$H_s = c_p T_1 (PR^{(\gamma-1)/\gamma} - 1)$$

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where c_p is the constant pressure heat capacity and γ is the ratio of the constant volume to constant pressure heat capacities. Output (useful fluid) power for the compressor is characterized by the isentropic compression power given by the product of m and H_s:

$$W_s = m H_s$$

A representative operating condition for the SSRB compressor with neon is

$T_1 =$ 284 K
PR = 1.71
m = 1.16 g/s
$p_1 =$ 1.1 atm
$f_s =$ 7738 rev/s

These values are determined from the SSRB cycle model given in [11], and are based on cryocooler operation with 5 watts of cooling at 65 K with a heat rejection temperature of 280 K. For this condition, the preceding equations give

$H_s = 70.0$ j/g
$W_s = 84.0$ watt

(For air with $T_1 = 293$ K, the same value of H_s would correspond to PR = 2.12).

A good indication of the eventual performance of the present breadboard components in neon is provided by the data points for which W_s is around 80 watts and f_s is around 7000-8000 rev/s. The inverter specification, which represents the design goal for the system, provides a benchmark for evaluating this performance. According to that specification, power input to the motor at the design point is

$$W_m = 175 \text{ watt}$$

making the overall compressor-motor efficiency equal to

$$W_s/W_m = 84.0 \div 175 = 0.48$$

Calculations of the inverter losses were given in Section 2.5 for $W_m = 175$ watt at the specified electrical parameters. This calculation can be corrected for the measured MOSFET R_{ds} as described in Section 3.2.2 to give

$$W_{inv} = W_{core} + W_{res} = 1.39 + 1.68 + 4.78 \times 0.60 = 5.9 \text{ watt}$$

resulting in the following for inverter input power and efficiency

$$W_0 = W_m + W_{inv} = 175 + 5.9 = 180.9 \text{ watt}$$

$$\eta_{inv} = W_m/W_0 = 175 \div 180.9 = 0.967$$

Overall power train efficiency is

$$\eta_s = W_s/W_0 = 84.0 \div 180.9 = 0.46$$

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In the spreadsheet calculations for each test point, W_s is determined from m, PR and T_1 as described above, W_0 is given by the product of V_0 and i_0, and W_{inv} is determined from i_{m0}, V_{m0} and f through Equations (12) and (13), where Equation (13) accounts for the measured MOSFET R_{ds}. In addition the motor power factor is calculated from the relation

$$\cos \theta = (2/3)\, W_m / (V_{m0}\, i_{m0})$$

Figure 27 displays the test results as a plot of inverter input power W_0 and isentropic compression power W_s for each test point, with the above design point and lines of constant η_s shown for reference. Most of the data points fall between the 0.15 and the 0.25 η_s lines. Data points near the design point W_s, which represent design point operation of the breadboard compressor, show W_0 values nearly two times the 180 watt design goal. This excess in W_0 is attributable mainly to high leakage and aerodynamic losses in the impeller, along with the additional motor and inverter losses incurred in carrying these excess impeller losses. As mentioned previously, the breadboard impeller design is preliminary and has not been optimized. Further development of the impeller is projected to reduce these losses, resulting in attainment of the η_s target. The impeller and motor losses are discussed in a test report presently being prepared under Contract NAS5-31281.

Figure 28 shows a plot of the calculated W_{inv} value vs. W_0 for each test point. The design point and lines of constant η_{inv} are shown for reference. The following proportionalities describe the trends in W_{inv} and η_{inv} over the test matrix:

$$W_{inv} \simeq i_{m0}^2 \simeq W_m^2 / (V_{m0} \cos \theta)^2$$

$$1 - \eta_{inv} = W_{inv} / W_0 \simeq W_m / (V_{m0} \cos \theta)^2$$

These were discussed in Section 2.5. W_{inv} is small enough that W_m and W_0 can be used interchangeably in describing trends in the data. At the data points for the design point isentropic compression power W_s (circled), the inverter operated close to the specified values of V_{m0} and cos θ, but W_0 was almost twice the design point value, as indicated above. This caused inverter losses to exceed the 6 watt design point value by approximately a factor of 4. Data points at the 180 watt design point inverter power correspond to speeds and isentropic compression powers that are much lower than the design point. Inverter loss exceeds the 6 watt design value at these data points as well, because the low electrical frequencies corresponding to the low speeds require the motor to run with lower V_{m0} values to avoid saturation. These lower V_{m0} values increase i_{m0} and the inverter loss. Trends in inverter loss and efficiency associated with V_{m0} and f are described further in the next few paragraphs.

Even though the low efficiency of the breadboard impeller caused the inverter loss to greatly exceed the 6 watt design point value, the inverter showed high efficiency over the full range of performance tests, falling between 90 and 95% as Figure 28 shows. The inverter will show its design point loss and efficiency once improvements in impeller performance allow it to operate simultaneously at its specified frequency voltage, current and power factor:

V_{m0} = 21.8 volt
i_{m0} = 10.7 amp
cos θ = 0.5

corresponding to W_m = 175 watt.

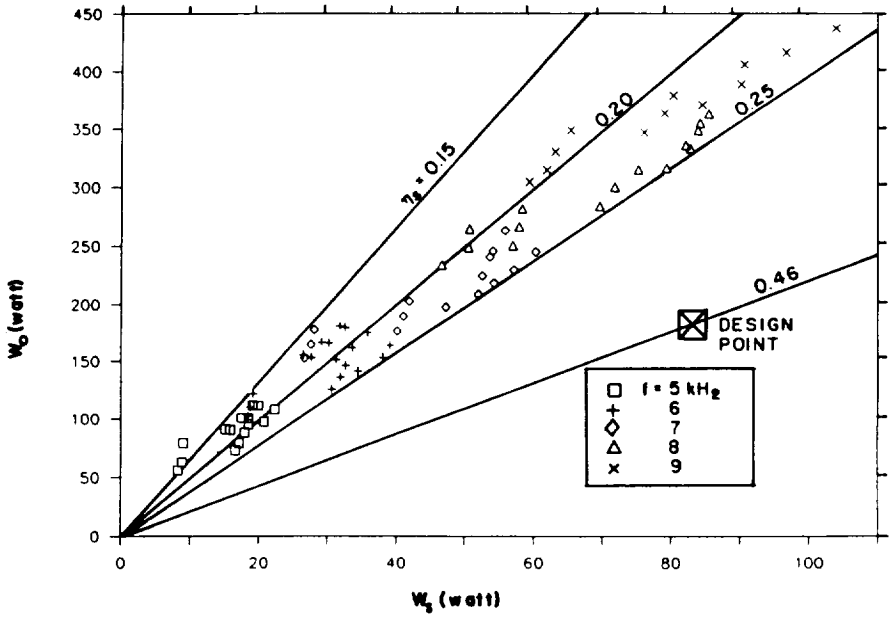

Figure 27. ISENTROPIC COMPRESSOR POWER (W_s) AND INVERTER INPUT POWER (W_o) FOR STEADY-STATE COMPRESSOR TEST POINTS AT INVERTER FREQUENCIES (f) OF 5-9 kHz

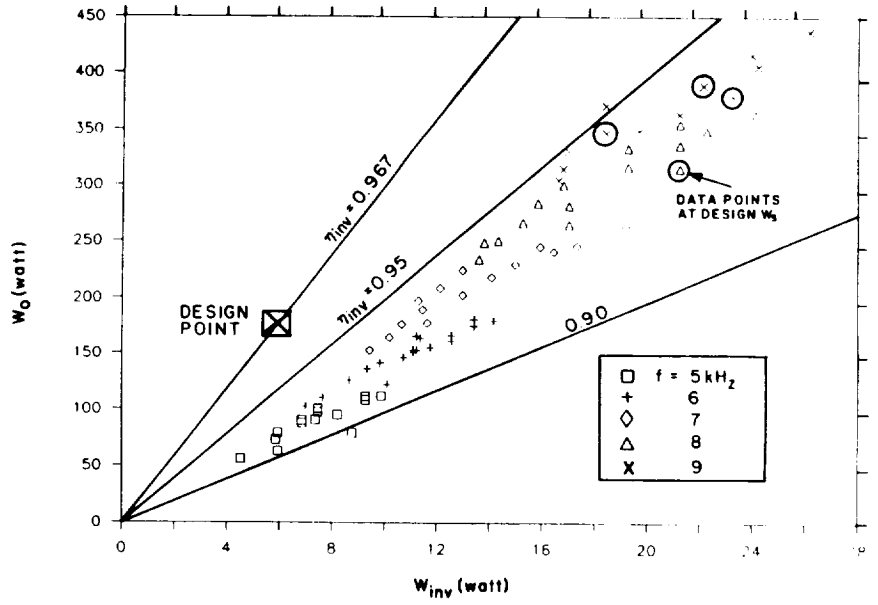

Figure 28. CALCULATED INVERTER LOSS (W_{inv}) AND INVERTER INPUT POWER (W_o) FOR STEADY-STATE COMPRESSOR TEST POINTS AT INVERTER FREQUENICES (f) OF 5-9 kHz

The data points at fixed f and throttle opening with different V_{m0} values, show subtle but interesting effects on performance. As V_{m0} is increased at fixed f and throttle, the motor magnetic field increases as long as it is below saturation. The increased magnetic field causes the shaft to speed up, decreasing s. An optimum value of V_{m0} can be expected which gives the highest possible motor efficiency for the fixed f and throttle opening. This is apparent from a consideration of what happens when V_{m0} is either too high or too low. If V_{m0} is too high, high stator currents needed to generate the corresponding high magnetic field lead to excessive resistance loss in the motor stator. If V_{m0} is too low, the slip can be excessively high, leading to high induced current and accompanying high resistance loss in the rotor. An even more important consequence of trying to operate with V_{m0} too low is the potential for stalling of the motor.

The groups of data points at fixed f and throttle opening in the tables of Appendix A show several examples of an optimum V_{m0} value, represented by maxima in both η_s and η_{inv}. Nearly all of the groups show a decrease in efficiency from saturation at high V_{m0}. To avoid stalling from excessive slip, caution was always exercised in decreasing V_{m0}. For some of the groups, this caution prevented the reaching of a low enough V_{m0} to get past the optimum point.

The influence of V_{m0} on motor performance is felt through its determination of the magnetic field, which scales with V_{m0}/f. An acceptable range of V_{m0}, over which the motor shows good efficiency, represents an acceptable range of magnetic field, extending from moderate slip at low magnetic field, to lower slip at higher magnetic field that is comfortably below saturation. Performance deteriorates at either excessive slip or saturation as stated above. Figure 29 shows a plot of V_{m0} vs. f for all of the test points, illustrating the upward trend of the V_{m0} range with f that is expected in view of the V_{m0}/f proportionality of the magnetic field.

The opposite extremes of high slip and magnetic saturation, which give rise to excessive motor loss, are represented by higher than optimum motor currents. For a given motor power, these higher than optimum currents naturally reduce the inverter efficiency. At the magnetic saturation extreme, high magnetizing current in the stator decreases the power factor ($\cos \theta$) to produce higher than optimum motor current. At the high slip extreme, the magnetic field is low so magnetizing current in the stator is low, resulting in higher power factor. Despite favorable power factor, higher than optimum motor current is produced by the low values of V_{m0}. Figure 30 shows a plot of power factor vs. slip for all of the test points. These data exhibit the monotonic trend of power factor with slip that has just been described.

3.2.4 Start-Up Tests

The breadboard compressor used for the steady-state performance tests ran on externally pressurized gas bearings. The bearings were pressurized prior to start-up so there was no starting friction for the motor and inverter to overcome. In all of those tests, the machine was started by slowly increasing V_0 with the inverter frequency set for 5 kHz.

Ultimately the compressor will run on self-acting tilt pad journal bearings. Dry contact between the shaft and the bearing pads at start-up results in a frictional force which must be overcome by the starting characteristics of the motor. In the absence of any large external radial loads on the shaft, this frictional force will be very small. The torque needed to overcome it should be much smaller than either the motor's operating torque at full speed or

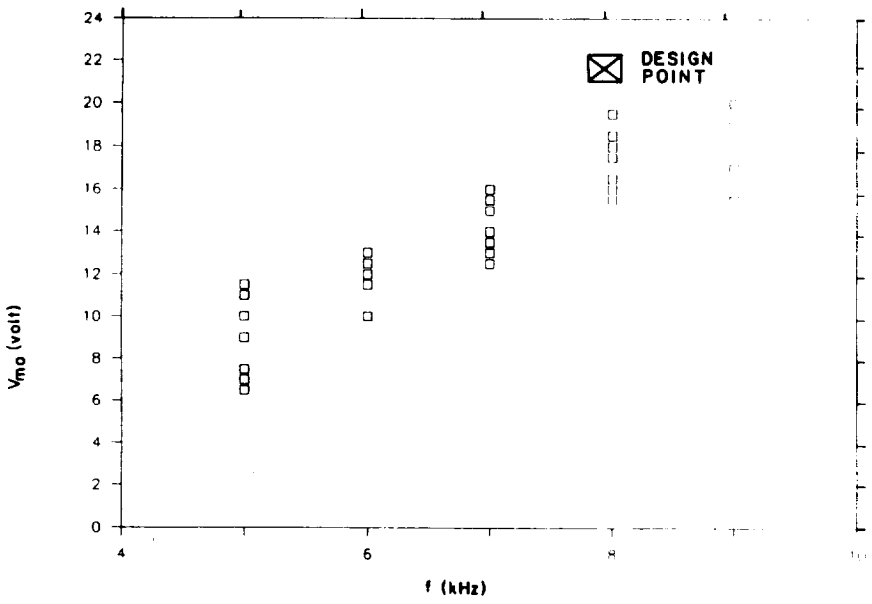

Figure 29. MOTOR VOLTAGE WAVEFORM AMPLITUDES (V_{mo}) AND INVERTER FREQUENCIES (f) FOR STEADY-STATE COMPRESSOR TEST POINTS

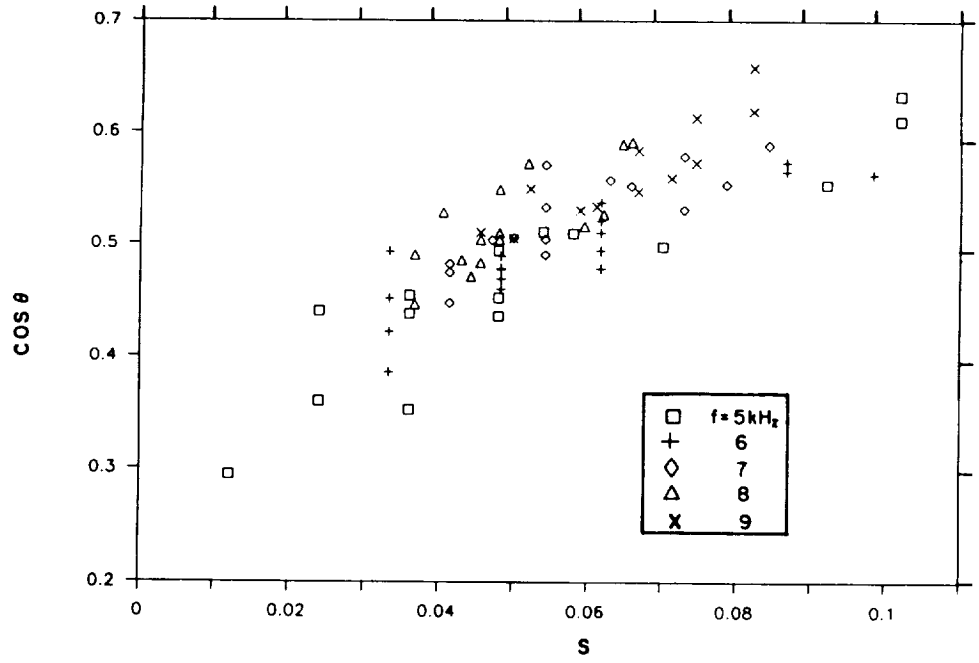

Figure 30. POWER FACTOR (cos θ) AND INDUCTION MOTOR SLIP (s) FOR STEADY-STATE COMPRESSOR THAT POINTS AT INVERTER FREQUENCIES (f) OF 5-9 kHz

the torque absorbed by acceleration of the shaft following lift-off. Although this frictional torque prior to lift-off may normally be very small, the initial current at start up can be substantial. At extremely low rotational speeds (high slip), the electrical impedance of the motor is at its minimum, resulting in high current, but the current is predominantly reactive, resulting in limited capability to produce torque. It is therefore important to ensure that the current needed to produce the required starting torque falls safely within the current ratings of the inverter MOSFET's.

Interest in the starting characteristics of the motor and inverter with tilt pad bearings has been further motivated by difficulties that had been encountered in the early development of the breadboard compressor [1]. In early tests performed with a commercial inverter, high radial forces from a permanent magnet thrust bearing prevented consistent smooth starting of the tilt pad bearings. The pressurized bearings were then implemented as an interim fix. A key objective of the present tests was to re-examine the compressor's starting characteristics with tilting pad bearings, given the new breadboard inverter, and given a thrust bearing that supplies a smaller radial force than the permanent magnet. Repeated smooth start-ups have been achieved, and peak starting currents drawn from the inverter have been modest, well within the ratings of the MOSFET's. These tests are described in the following paragraphs.

The tilt pad bearings and the new thrust bearings used for the start-up tests were fabricated under the concurrent SSRB cryocooler development project (Contract NAS5-31281). The start-up tests to verify the starting current capability of the inverter were performed under the present inverter project. Further related tests, focusing on the influences of rotational speed and thrust bearing parameters on stability of the tilt pad bearings, were performed under the SSRB project. Results of those tests are described in the test report for that project.

The start-up tests were run with two different compressor assemblies. The first assembly was the same one used for the steady-state tests, except that tilt pad bearings replaced the pressurized bearings and an electromagnet replaced the thrust bearing's permanent magnet. The electromagnet could be operated with reduced current at start-up to provide a much lower radial load on the shaft against the tilt pad bearings than the permanent magnet had provided. The second assembly was essentially a duplicate machine. Its impeller contained a self-acting spiral groove thrust bearing for comparative testing.

No significant difference was observed between the two assemblies in terms of start-up behavior of the motor and inverter. The bulk of the tests, consisting of to to 30 repeated starts, were performed with the first assembly. For each of these 20 to 30 starts, the inverter frequency f was set for 3 kHz, the DC voltage $V_0$was set for 8 volts, 5 volts DC were applied to the thrust bearing coil, and the throttle was moderately open. Based on visual observation of the digital multimeter, the DC current i_0 would appear to reach a peak of approximately 8 to 10 amps, and then fall off rapidly as the shaft accelerated, stabilizing at 5 amps at a rotational speed just under 3000 rev/s. Because of the short duration of this process, it was not possible to get a more accurate visual reading of the peak current. The 8 volt - 3 kHz starting condition for these tests does not necessarily represent an optimum starting condition for the machine. It was a conservative choice for initial tests with the tilt pad bearings. It may be feasible and advantageous eventually to use a higher starting frequency.

Given the uncertainty in the measurement of the peak starting current, locked rotor tests were conducted to determine the maximum current that the motor can draw when started with a particular voltage and frequency. In the locked rotor test, the rotor is held stationary to enable current to be measured at the point of minimum motor impedance (zero speed). Since this minimum impedance is predominantly reactive, current should be proportional to the voltage-frequency ratio V_0/f. Torque on the locked rotor can be shown to be proportional to the square of the motor current and inversely proportional to frequency.

In an actual start-up, the shaft would start spinning instantly if the locked rotor torque corresponding to the starting values of V_0 and f exceeds the frictional torque The locked rotor current would only exist momentarily. Its duration would depend on how rapidly the shaft accelerates. If the frictional torque exceeds the locked rotor torque, the locked rotor current would flow indefinitely and the shaft would not spin. To start successfully, the locked rotor torque would have to be increased by either increasing V_0 or decreasing f. To increase the locked rotor torque without increasing the locked rotor current, f is decreased while holding V_0/f constant. In this regard, the cautious approach of starting the compressor at reduced frequency reflects a desire to achieve a conservatively high starting torque for a given current. Starting at 8 kHz might be possible. The locked rotor current would be higher for the same torque, and the feasibility remains to be explored.

Locked rotor current was measured at frequencies of 3, 4 and 5 kHz, at V_0/f ratios up to 2 volt/kHz. Measured values of i_0 and i_{m0} are plotted as functions of V_0/f in Figures 31 and 32. The 8 to 10 amp peak DC currents that were observed during the actual start-up tests can be seen from Figure 31 to correspond to a V_0/f value of approximately 1 volt/kHz. The V_0/f value for the start-up tests, however, was 2.667 volt/kHz, which would, from an extrapolation of Figure 31, result in a locked rotor DC current on the order of 25 to 30 amps. That currents this high were not seen during the start-up tests is evidence that the starting torque was more than adequate to instantly overcome friction and accelerate the rotor.

From Eqs. (16) to (18) with $N_{sa}/N_{pa} = 2/3$ and $N_{sb}/N_{pb} = 1/2$, the peak primary lead current is given by

$$i_{p0} = 0.601 \times i_{m0}$$

Since i_p flows for 50% of the time through each MOSFET switch and since each switch consists consists of two MOSFET's in parallel, the rms current through each MOSFET can be shown to equal $i_{p0}/4 = 0.150 \times i_{m0}$. Therefore, under the most severe locked rotor test condition (V_0/f = 2 volt/kHz, f = 5 kHz), the measured i_{m0} value of 28 amps corresponds to only 4.2 amps-rms in each MOSFET, safely below the 20 to 28 amp continuous current rating of the IRF540 MOSFET's. From an extrapolation of Figure 32, the locked rotor condition for the actual start-up tests, had it been realized, would have resulted in approximately i_{m0} = 40 amps, for which the MOSFET rms currents would have been 6 amps, still a safe value.

From the standpoint of the inverter, the most conservative way to start the motor is to limit the starting V_0/f value to a level for which the MOSFET currents for a locked rotor are conservative. If the motor is able to accelerate quickly enough that the locked rotor current is not realized, as was evident from the start-up tests, it may be possible to use less conservative V_0/f values (still keeping V_0/f below the level that would saturate the motor or the inverter transformers), enabling a higher starting frequency to be used while maintaining a conservative starting torque level. Ideally, to keep the controls as simple as possible, it would be most desirable to start the motor at its 8 kHz design frequency.

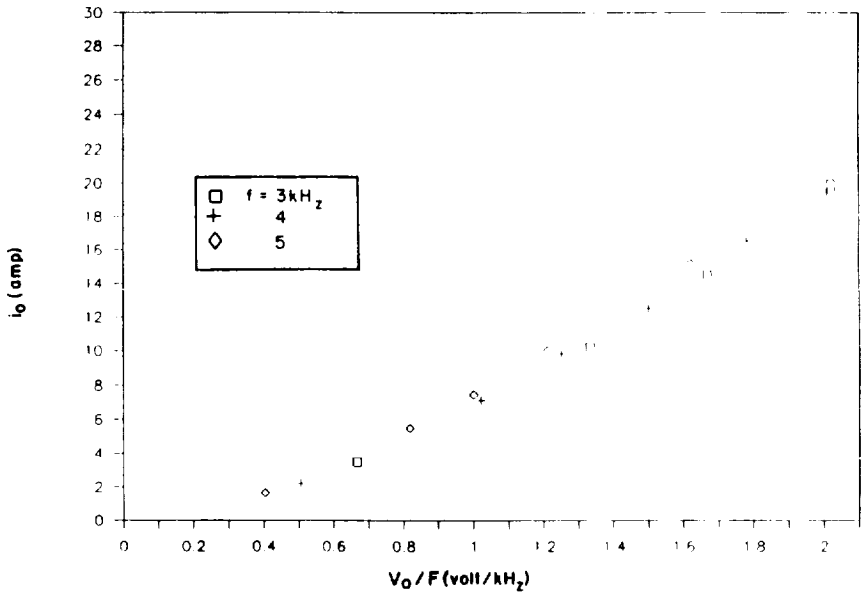

Figure 31. DC CURRENT (i_o) AND DC VOLTAGE-FREQUENCY RATIO (V_o/f) FOR LOCKED ROTOR TEST AT INVERTER FREQUENCIES (f) OF 3, 4 AND 5 kHz.

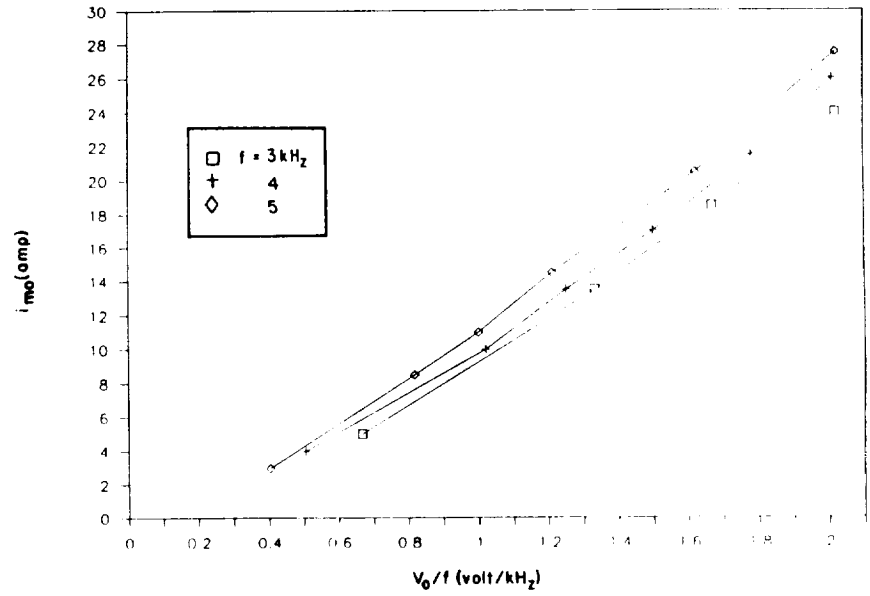

Figure 32. MOTOR CURRENT WAVEFORM AMPLITUDE (i_{mo}) AND DC VOLTAGE-FREQUENCY RATIO (V_o/f) FOR LOCKED ROTOR TEST AT INVERTER FREQUENICES (f) OF 3, 4 AND 5 kHz.

4. PRELIMINARY DESIGN OF ENGINEERING MODEL

Effort on design of the inverter engineering model was coordinated with the preliminary design of the SSRB cryocooler performed under Contract NAS5-31281. Current plans call for the fabrication of an inverter engineering model under a future phase of that contract. Scope of the present design effort included the development of a packaging concept, preparation of preliminary fabrication drawings for the package, and the selection of MIL-standard or S-class equivalents for the key switching circuit components.

Guiding principles for the engineering model design were to develop a package that could attach directly to the compressor housing for cooling, and to make use of the successful electronic component arrangement of the breadboard inverter. The natural circular arrangement of the transformers and MOSFET's is well suited to a cylindrical package attachable to an end face of the compressor housing. Based on the configuration of the breadboard with some minor tightening up of the transformer and MOSFET positioning, a cylindrical envelope of 6.75 inch diameter by 4.1 inch length was defined. Figure 33 shows this envelope attached to one end of the compressor housing, and shows the arrangement of the transformers and circuit board within the envelope. The arrangement provides thermally conducting paths to carry the inverter losses from the transformers and MOSFET's to the compressor housing which is cooled by the spacecraft thermal bus. Details of the thermal and electrical packaging will be discussed below.

The only significant change from the breadboard electronics is the substitution of a single IR2N764 MOSFET for the two paralleled IRF540 MOSFET's at each switch. The IR2N764 is available in JANTX and JANTXV designations, qualified to MIL-S-19500/543. It has a TO-3 style package, providing greater ruggedness and more surface area for heat conduction than the TO-220 package of the IRF540. The maximum current rating is 38 amp, compared with 28 amp for the IRF540. R_{ds} is specified at 0.055 Ω, compared with 0.077 ÷ 2 = 0.039 Ω for the parallel IRF540 pair. MOSFET loss is 41% higher but reliability is enhanced by using half the number of individual MOSFET's.

The IR2110 MOSFET drivers fortunately appear well suited to the engineering model and future flight versions of the inverter. This chip is manufactured in a ceramic package and can be screened to MIL-STD-883. In discussions with International Rectifier it was determined that this component is presently being screened for S-Class.

In the engineering model, the array of six D-type flip flops will be provided by three 4013 dual D-type flip-flop chips. The 4013 is available as an S-class component. Several versions of the 555 timing chip are available in various MIL classifications. The version most readily upgradable to S-Class has not been identified at this stage of the design process.

Figure 34 shows a mechanical layout of the inverter. Table 4 is a preliminary Materials and Parts List that accompanies the layout. The circular circuit board sits above the toroidal transformers in the manner of the breadboard inverter. The board consists of a single layer printed circuit board backed by an aluminum heat sink plate of 0.090 inch thickness. The heat sink plate is on the underside of the board, facing the transformers. The twelve MOSFET's are mounted directly to the heat sink plate, which places them underneath the PC board as shown in Figure 34. The remaining components are mounted to the top side of the PC board. The IR2110 driver chips are positioned directly above the MOSFET's. The three 4013 D-type flip-flop chips and the 555 timing chip are positioned in the center of the board.

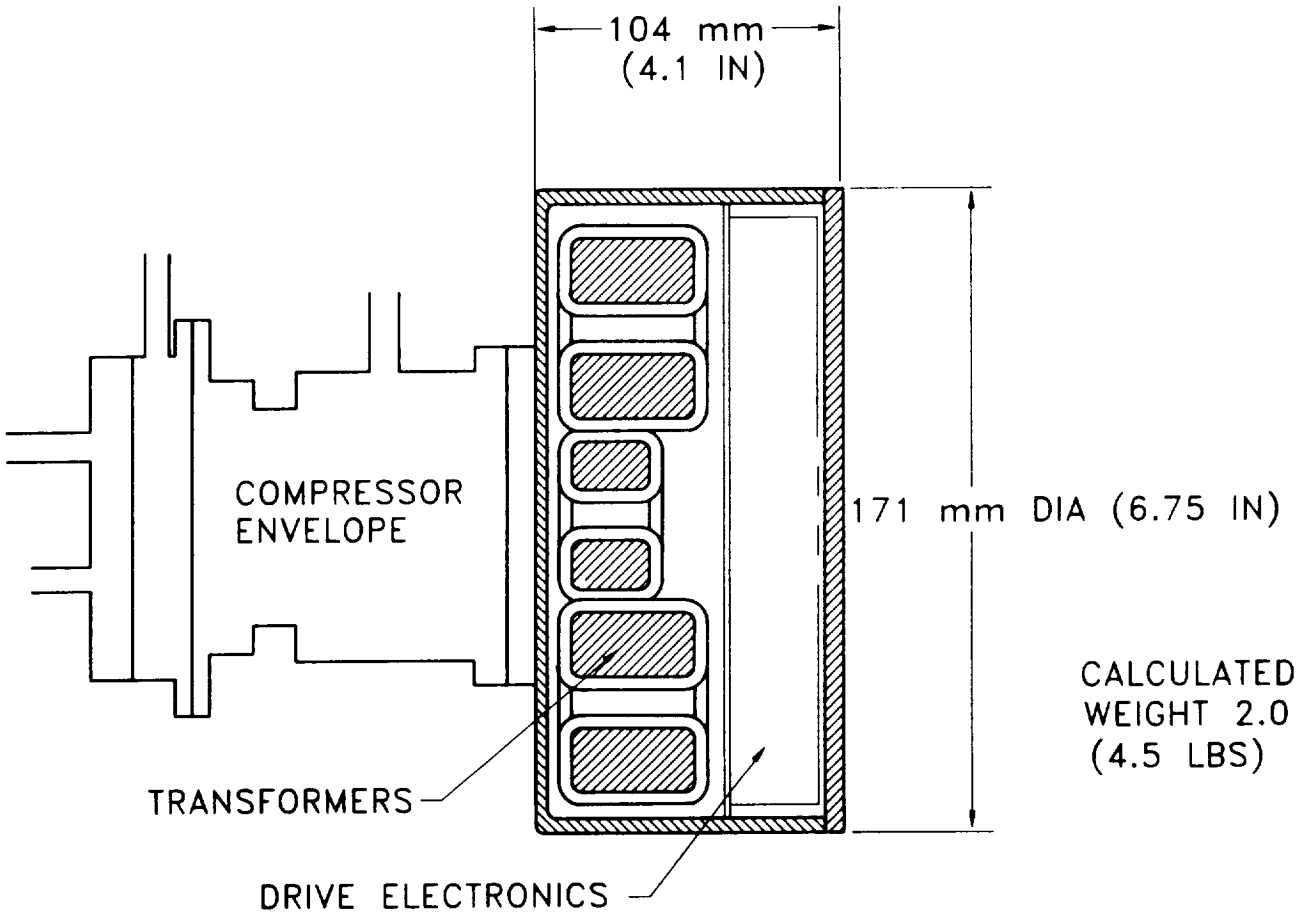

Figure 33. ENVELOPES OF COMPRESSOR AND ENGINEERING MODEL INVERTER

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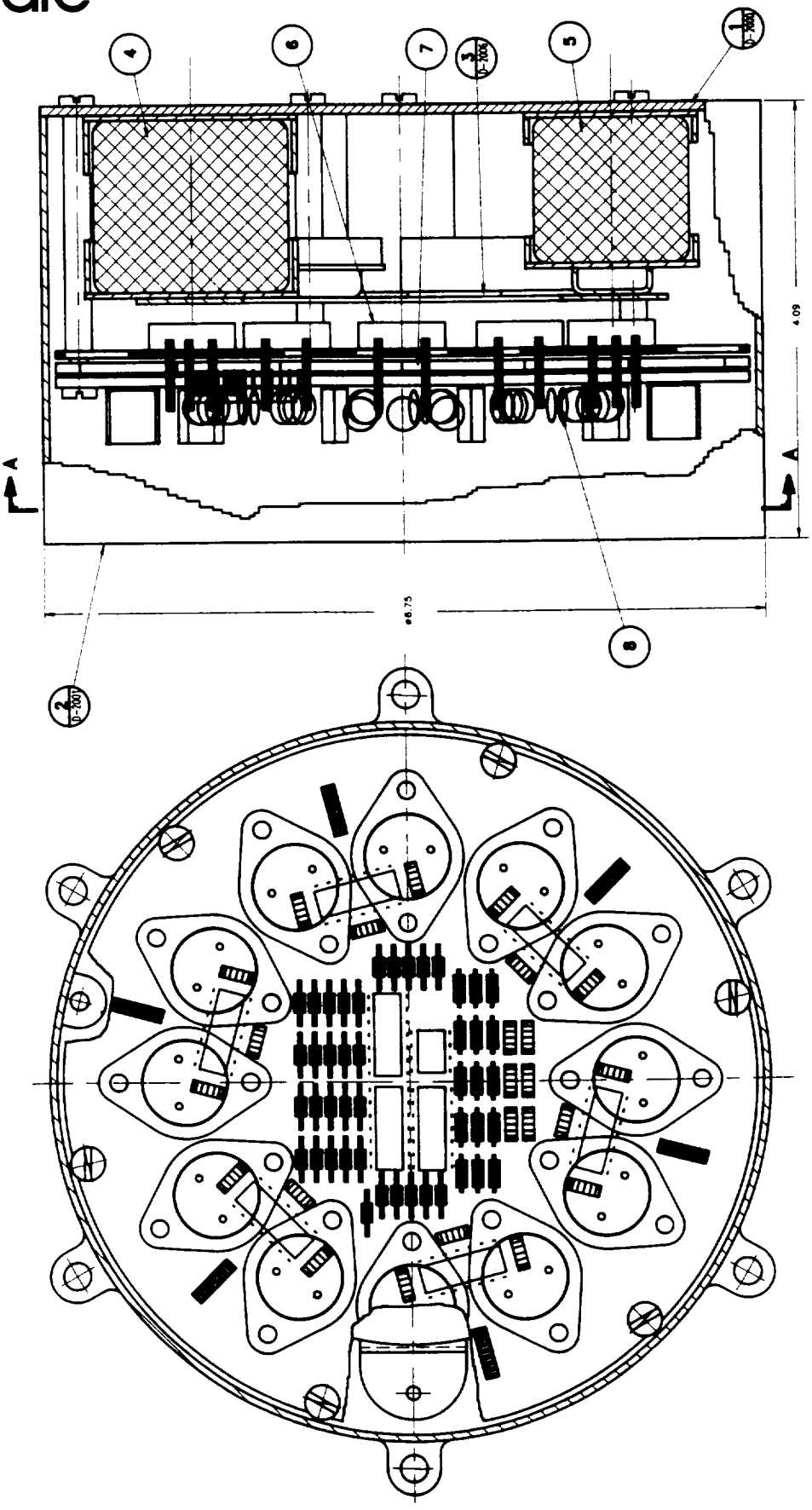

Figure 34. LAYOUT OF ENGINEERING MODEL INVERTER DESIGN

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Table 4. MATERIALS AND PARTS LIST

Preliminary Materials and Processes for Inverter (D-6836-2009)

Assembly Find No.	Part or Subassembly	Identification or Drawing No.	Materials and Treatment	Manufacturing Process	Inspections	Tests
1	Base Plate	D-6836-2000	Aluminum Anodize	Machining Fastening	1. Receiving 2. Dimensional tolerance	None
2	Cover	D-6836-2001	Aluminum Anodize	Machining Fastening Forming	1. Receiving 2. Dimensional tolerance	None
3	Top Plate Assembly	D-6836-2006	Aluminum Anodize	Machining Fastening Forming	1. Receiving 2. Dimensional tolerance	None
4 & 5	Transformer	See Below Item 3-5	Ferrite PTFE Copper Wire	Winding	1. Receiving	Continuity
6	Transistor	MIL-S-19500		Fastening Soldering	1. Receiving 2. Dimensional tolerance	Verification
7	Heat Sink	TBD	Aluminum	Machining	1. Receiving 2. Dimensional tolerance	None
8	Circuit Board	TBD	Polyimide-Glass Electronics** Solder-Sn63 Pb37	Assembly Soldering	1. Receiving 2. Dimensional tolerance	Verification

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The inverter housing consists of an aluminum base plate which attaches to the compressor housing and to which the transformers and PC board are structurally and thermally attached, and a cylindrical aluminum cover plate. The PC board is attached to the base plate through six aluminum stand-off rods at the periphery of the board which provide thermal conduction to the base plate. Each transformer is held to the base plate through a pair of aluminum covers that fits over each end of the transformer. A hold-down ring clamps the six upper transformer covers to the base plate. The lower transformer covers conduct heat directly to the base plate. The upper covers conduct heat to the base plate through the hold-down ring. Weight of the complete inverter assembly has been estimated to be 2.0 kg.

Logic circuitry that will execute the start-up sequence described in Section 2.7 has not been defined at this preliminary design stage. That circuitry would consist strictly of low power logic components that could be mounted on a second circular board that would be positioned above the main board through similar stand-off rods. A second board might require a minimal lengthening of the cylindrical envelope. Also remaining to be defined is a DC-to-DC converter to regulate the DC voltage supplied to the inverter from the spacecraft bus. Options include an off-the-shelf converter that would be a separate module of the cryocooler, or a custom designed converter that could be integrated into the inverter package. The converter, along with the start-up logic will be addressed in a future phase of the SSRB cryocooler development under Contract NAS5-31281.

In conclusion, it should be noted that this preliminary design of the engineering model reflects the conservative design of the breadboard. Reduction in power levels through improvement of the compressor efficiency and the use of higher performance magnetic materials present a significant opportunity for reduction of the transformer sizes and consequent shrinking and weight reduction of the inverter package.

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5. CONCLUSIONS AND RECOMMENDATIONS

The overall objective of developing and demonstrating the performance of a high frequency inverter for miniature motors was definitively met during this project. Specific performance objectives in driving a miniature centrifugal compressor were exceeded.

The inverter design is based on a unique topology for a transformer coupled inverter. A straightforward design methodology was developed through which inverters can be sized for a wide range of applications and operating conditions. As a result of extensive measurement and analysis, waveform details and loss mechanisms are well understood and highly predictable.

The inverter topology uses six transformers and twelve MOSFET switches to generate stepped AC voltage waveforms. Through proper selection of transformer turns ratios, all harmonics below the eleventh can be eliminated. The breadboard inverter developed under this project has a design point efficiency of 96.7% at a frequency of 8 kHz and an output power of 175 watt.

Starting currents drawn by the compressor's induction motor were measured and are well within the current ratings of the MOSFET switches.

The inverter is an open-loop system with minimal control requirement. Key control variables are input DC voltage, which will be fixed by a pre-regulator, and frequency, which will be fixed by a potentiometer setting in a simple timing circuit.

The overall recommendation is to proceed with the development of an engineering model inverter in conjunction with NASA's on-going development program for the reverse-Brayton cryocooler. The existing breadboard inverter can be used in its present state for upcoming testing of a complete breadboard cryocooler.

Development effort for an engineering model should focus on electronics packaging for eventual flight qualification, an efficient pre-regulator if mission requirements mandate that the inverter operate from an unconditioned DC bus, and control logic for the start-up sequence. Further tests need to be conducted in parallel with development of the compressor's bearing system to determine the optimum voltage and frequency for start-up.

Prospects for high reliability over a 5-10 year mission life in space are excellent based on the following:

- Small number of electronic components (12 discrete MOSFETS, 9 integrated circuit elements).
- MOSFET currents for normal operation are within 20% of rated currents.
- All electronic components in engineering model design are available in S-class or with comparable MIL qualifications.

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A quantitative reliability analysis, which was beyond the scope of the present program, should be performed in conjunction with the engineering model development effort. Additionally, an assessment should be made of the structural design of the inverter in terms of its durability under anticipated launch loads.

Since performance objectives for the inverter have been exceeded in the present breadboard development effort, no further performance development is needed. The design can readily be modified, by adjusting the transformer turns ratios, to accommodate different DC bus voltage levels associated with different mission requirements. Operation at higher DC voltage levels will tend to improve the inverter efficiency.

It may be possible to reduce the weight of the inverter transformers, by replacing the present ferrite cores with high performance magnetic alloys. This should be investigated as part of the engineering model effort.

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APPENDIX A

COMPRESSOR TEST DATA AND PERFORMANCE CALCULATIONS

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Table A-1. Compressor Test Data for f = 5 kHz Measurements

Date	f	pa	pa
	kHz	mm-Hg	psi
2/13/91	5	740	14.309

V0	i0	fs	2*Vm0	2*im0	T1	T2	Tfm	p1	p2	pfm	Q
volt	amp	kHz	volt	amp	C	C	C	psig	psig	psig	cfm
15	6.34	4.88	23	28	21.6	33.5	21.8	0	4.94	4.83	0.96
12	6.6	4.76	18	24	21.6	36.5	21.6	0	4.65	4.55	0.95
10	7.3	4.65	15	24	21.1	24.4	16.9	0	4.51	4.41	0.94
15	5.28	4.94	22	29	21.1	26.9	17.1	0	5.22	5.18	0.43
12	5.25	4.82	18	24	22.4	31.4	17.7	0	5.03	4.98	0.44
10	5.6	4.76	15	21	22.9	30.3	18.5	0	4.74	4.71	0.44
14	7.73	4.88	20	30	19.6	26.5	15.6	0	3.64	3.41	1.63
12	8.12	4.76	18	27	18.7	26.3	15.1	0	3.45	3.23	1.61
10	8.79	4.54	15	26	18.6	24.6	14.2	0	3.12	2.92	1.55
14	7.96	4.82	20	30	18	25.5	13.1	0	3.02	2.75	1.79
12	8.36	4.71	18	27	17.2	26.1	13.5	0	2.85	2.6	1.78
10	9.02	4.49	14	26	17.9	25.2	13.8	0	2.57	2.35	1.7
14	7.98	4.82	20	31	17.2	27.6	13.6	0	2.81	2.54	1.87
12	8.38	4.73	18	27	16.8	27.2	14	0	2.64	2.39	1.83
10	9.07	4.49	13	27	17.3	24.8	13.5	0	2.39	2.16	1.76

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Table A-2. Compressor Test Data for f = 5 kHz Performance Calculations

Date	f											
	kHz											
2/13/91	5											
m	PR	Hs	Ws	WO	etas	Wcore	Wres	Winv	Wm	etainv	cos	slip
g/s		j/g	watt	watt		watt	watt	watt	watt		(theta)	
0.71	1.35	26.2	18.5	95.1	0.194	0.43	7.76	8.19	86.9	0.914	0.36	0.0240
0.69	1.32	24.8	17.1	79.2	0.216	0.24	5.70	5.95	73.3	0.925	0.45	0.0480
0.69	1.32	24.1	16.6	73.0	0.227	0.15	5.70	5.86	67.1	0.920	0.50	0.0700
0.33	1.36	27.5	9.0	79.2	0.114	0.43	8.33	8.76	70.4	0.889	0.29	0.0120
0.33	1.35	26.7	8.8	63.0	0.140	0.24	5.70	5.95	57.1	0.906	0.35	0.0360
0.33	1.33	25.3	8.2	56.0	0.147	0.15	4.37	4.52	51.5	0.919	0.44	0.0480
1.13	1.25	19.7	22.3	108.2	0.206	0.36	8.91	9.27	98.9	0.914	0.44	0.0240
1.11	1.24	18.7	20.7	97.4	0.213	0.24	7.22	7.46	90.0	0.923	0.49	0.0480
1.05	1.22	17.0	17.9	87.9	0.204	0.15	6.69	6.85	81.1	0.922	0.55	0.0920
1.21	1.21	16.4	19.9	111.4	0.178	0.36	8.91	9.27	102.2	0.917	0.45	0.0360
1.19	1.20	15.5	18.5	100.3	0.184	0.24	7.22	7.46	92.9	0.926	0.51	0.0580
1.12	1.18	14.1	15.8	90.2	0.175	0.15	6.69	6.85	83.4	0.924	0.61	0.1020
1.25	1.20	15.3	19.1	111.7	0.171	0.36	9.51	9.87	101.8	0.912	0.44	0.0360
1.21	1.18	14.4	17.4	100.6	0.173	0.24	7.22	7.46	93.1	0.926	0.51	0.0540
1.15	1.17	13.2	15.1	90.7	0.166	0.15	7.22	7.37	83.3	0.919	0.63	0.1020

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Table A-3. Compressor Test Data for f = 6 kHz Measurements

Date	f	pa	pa
	kHz	mm-Hg	psi
2/13/91	6	740	14.309

V0	i0	fs	2*Vm0	2*im0	T1	T2	Tfm	p1	p2	pfm	Q
volt	amp	kHz	volt	amp	C	C	C	psig	psig	psig	cfm
18	10.06	5.71	26	36	17.4	37.3	15.1	0	4.01	3.63	2.11
16	10.41	5.63	23	35	16.9	35.3	15.2	0	3.8	3.44	2.06
14	11.1	5.41	20	34	16.9	34.6	14.3	0	3.57	3.23	2
18	9.98	5.71	25	37	17.1	36.9	14.3	0	4.23	3.87	2.03
16	10.37	5.63	24	33	16.8	36.5	13.9	0	4.04	3.7	1.98
14	10.94	5.48	20	33	17	35.2	14.7	0	3.76	3.42	1.97
18	9.72	5.71	26	36	16.7	37.9	14.4	0	4.93	4.61	1.87
16	10.1	5.63	23	35	17.2	37	14.1	0	4.72	4.4	1.84
14	10.8	5.48	20	33	17.4	35.4	13.9	0	4.44	4.14	1.83
18	9.1	5.8	25	33	17.3	35.4	14.2	0	6.4	6.12	1.49
16	9.57	5.63	24	33	17.1	35.4	14.6	0	6.2	5.94	1.51
14	10.1	5.48	20	31	17.2	33.8	14.6	0	5.79	5.54	1.48
18	8.12	5.8	25	32	17.1	33.5	14.4	0	7.13	6.95	1.09
16	8.5	5.71	24	30	17.5	32.8	13.7	0	6.97	6.79	1.09
14	8.97	5.63	20	29	18	31.6	14	0	6.63	6.46	1.11
18	6.79	5.8	25	31	18.7	29.4	15.5	0	7.46	7.36	0.6
16	6.88	5.8	24	27	18.8	29.2	15.4	0	7.32	7.22	0.6
14	7.31	5.71	20	26	19	27.4	15.4	0	7.14	7.05	0.61

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Table A-4. Compressor Test Data for f = 6 kHz Performance Calculations

page 2

Date 2/13/91 — f 6 kHz

m g/s	PR	Hs j/g	Ws watt	WO watt	etas	Wcore watt	Wres watt	Winv watt	Wm watt	etainv	cos (theta)	slip
1.49	1.28	21.3	31.8	181.1 -	0.175	0.58	12.83	13.41	167.7	0.926	0.48	0.0483
1.44	1.27	20.3	29.2	166.6	0.175	0.43	12.13	12.56	154.0	0.925	0.51	0.0617
1.38	1.25	19.1	26.5	155.4	0.170	0.31	11.44	11.75	143.6	0.924	0.56	0.0983
1.46	1.30	22.4	32.6	179.6 -	0.181	0.58	13.55	14.14	165.5	0.921	0.48	0.0483
1.41	1.28	21.4	30.2	165.9	0.182	0.43	10.78	11.21	154.7	0.932	0.52	0.0617
1.38	1.26	20.1	27.6	153.2	0.180	0.31	10.78	11.09	142.1	0.928	0.57	0.0867
1.40	1.34	25.7	35.8	175.0	0.205	0.58	12.83	13.41	161.5	0.923	0.46	0.0483
1.36	1.33	24.7	33.6	161.6	0.208	0.43	12.13	12.56	149.0	0.922	0.49	0.0617
1.33	1.31	23.4	31.2	151.2	0.207	0.31	10.78	11.09	140.1	0.927	0.57	0.0867
1.20	1.45	32.5	39.0	163.8	0.238	0.58	10.78	11.36	152.4	0.931	0.49	0.0333
1.21	1.43	31.6	38.0	153.1	0.248	0.43	10.78	11.21	141.9	0.927	0.48	0.0617
1.16	1.40	29.7	34.4	141.4	0.243	0.31	9.51	9.82	131.6	0.931	0.57	0.0867
0.91	1.50	35.7	32.6	146.2	0.223	0.58	10.14	10.72	135.4	0.927	0.45	0.0333
0.91	1.49	35.0	31.9	136.0	0.234	0.43	8.91	9.34	126.7	0.931	0.47	0.0483
0.91	1.46	33.6	30.6	125.6	0.244	0.31	8.33	8.63	116.9	0.931	0.54	0.0617
0.51	1.52	37.3	19.1	122.2	0.156	0.58	9.51	10.10	112.1	0.917	0.39	0.0333
0.51	1.51	36.7	18.6	110.1	0.169	0.43	7.22	7.65	102.4	0.931	0.42	0.0333
0.51	1.50	36.0	18.4	102.3	0.180	0.31	6.69	7.00	95.3	0.932	0.49	0.0483

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Table A-5. Compressor Test Data for f = 7 kHz Measurements

Date	f	pa	pa
	kHz	mm-Hg	psi
2/13/91	7	740	14.309

V0	i0	fs	2*Vm0	2*im0	T1	T2	Tfm	p1	p2	pfm	Q
volt	amp	kHz	volt	amp	C	C	C	psig	psig	psig	cfm
22	8.08	6.71	30	33	20.2	35.7	16.4	0	10.1	9.9	0.61
20	8.23	6.71	28	31	18.6	37	14.8	0	9.93	9.79	0.61
18	8.49	6.62	26	30	18.9	34.9	15.6	0	9.69	9.53	0.61
22.03	9.2	6.71	30	35	19.9	38	15.6	0	9.91	9.71	0.93
20.04	9.46	6.62	27	33	19.4	39.4	16.3	0	9.7	9.5	0.94
18	9.8	6.54	25	32	19.7	39	16.3	0	9.36	9.17	0.96
22	10.2	6.67	32	35	18.1	42.2	15.2	0	9.49	9.24	1.24
20	10.44	6.62	27	34	19.5	40.3	15.3	0	9.31	9.05	1.25
18	10.98	6.49	26	33	17.5	41.2	15.2	0	8.9	8.65	1.21
22	11.14	6.65	31	39	17	46.1	14.7	0	8.94	8.6	1.54
20	11.48	6.56	27	38	16.1	43.7	14.8	0	8.67	8.35	1.52
18	12.13	6.41	25	37	17	41.8	12.4	0	8.28	7.96	1.51
22	11.96	6.62	30	43	15	43	14.7	0	7.17	6.75	1.89
20	12.29	6.49	28	41	16.2	42.7	13.1	0	6.86	6.46	1.91
19	12.67	6.45	27	40	15.9	42.4	12.2	0	6.74	6.35	1.93

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Table A-6. Compressor Test Data for f = 7 kHz Performance Calculations

page 2

Date: 2/13/91 — f: 7 kHz

m g/s	PR	Hs j/g	Ws watt	WO watt	etas	Wcore watt	Wres watt	Winv watt	Wm watt	etainv	cos (theta)	slip
0.58	1.71	48.6	28.1	177.8	0.158	0.85	10.78	11.63	166.1	0.935	0.45	0.0414
0.58	1.69	47.6	27.6	164.6	0.168	0.67	9.51	10.18	154.4	0.938	0.47	0.0414
0.57	1.68	46.7	26.7	152.8	0.175	0.51	8.91	9.42	143.4	0.938	0.49	0.0543
0.88	1.69	47.8	41.9	202.7	0.207	0.85	12.13	12.98	189.7	0.936	0.48	0.0414
0.88	1.68	46.8	41.1	189.6	0.217	0.67	10.78	11.45	178.1	0.940	0.53	0.0543
0.88	1.65	45.5	40.2	176.4	0.228	0.51	10.14	10.65	165.8	0.940	0.55	0.0657
1.15	1.66	45.8	52.6	224.4	0.234	0.85	12.13	12.98	211.4	0.942	0.50	0.0471
1.15	1.65	45.2	51.9	208.8	0.249	0.67	11.44	12.11	196.7	0.942	0.57	0.0543
1.09	1.62	43.3	47.3	197.6	0.239	0.51	10.78	11.29	186.3	0.943	0.58	0.0729
1.39	1.62	43.3	60.2	245.1	0.246	0.85	15.06	15.91	229.2	0.935	0.51	0.0500
1.36	1.61	42.1	57.1	229.6	0.249	0.67	14.30	14.96	214.6	0.935	0.56	0.0629
1.34	1.58	40.6	54.2	218.3	0.248	0.51	13.55	14.06	204.3	0.936	0.59	0.0843
1.57	1.50	35.6	55.8	263.1	0.212	0.85	18.31	19.15	244.0	0.927	0.50	0.0543
1.57	1.48	34.4	54.1	245.8	0.220	0.67	16.64	17.31	228.5	0.930	0.53	0.0729
1.58	1.47	33.8	53.6	240.7	0.223	0.58	15.84	16.42	224.3	0.932	0.55	0.0786

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Table A-7. Compressor Test Data for f = 8 kHz Measurements

Date	f	pa	pa
	kHz	mm-Hg	psi
2/14/91	7.9	727	14.058

V0	i0	fs	2*Vm0	2*im0	T1	T2	Tfm	p1	p2	pfm	Q
volt	amp	kHz	volt	amp	C	C	C	psig	psig	psig	cfm
26	10.18	7.61	37	40	17.6	44	13.6	0	13.06	12.84	0.79
24	10.37	7.58	33	36	17.7	43.5	13.7	0	12.91	12.69	0.8
22	10.63	7.52	32	36	18	42.6	13.5	0	12.6	12.39	0.76
26	10.83	7.61	36	40	17.1	46.5	14	0	12.76	12.52	0.94
24	11.1	7.54	35	38	17.7	42.4	12.2	0	12.71	12.46	0.93
22	11.39	7.43	33	37	17.2	40.8	12.5	0	12.37	12.13	0.95
26	12.12	7.55	37	45	16.6	48.1	12.4	0	12.29	11.97	1.27
24	12.51	7.49	33	40	16.9	47.4	11.7	0	12.04	11.72	1.24
22	12.91	7.38	31	39	16.7	46.2	11.6	0	11.61	11.3	1.26
26	12.92	7.52	37	45	15.6	52	11.7	0	11.78	11.4	1.47
24	13.19	7.41	35	43	15.6	51.3	12.2	0	11.41	11.04	1.48
27	12.91	7.56	39	46	15.6	53.2	11.9	0	11.87	11.48	1.49
27	13.45	7.54	39	48	15.6	53.3	11.9	0	11.03	10.59	1.67
26	13.65	7.52	36	45	15.5	52.7	11.7	0	10.95	10.51	1.66
24	13.88	7.39	33	43	15.5	52.1	11.8	0	10.6	10.17	1.7

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Table A-8. Compressor Test Data for f = 8 kHz Performance Calculations

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Date	f kHz
2/14/91	7.9

m g/s	PR	Hs j/g	Ws watt	W0 watt	etas	Wcore watt	Wres watt	Winv watt	Wm watt	etainv	cos (theta)	slip
0.84	1.93	60.3	50.7	264.7	0.191	1.17	15.84	17.01	247.7	0.936	0.45	0.0367
0.85	1.92	59.8	50.6	248.9	0.203	0.95	12.83	13.78	235.1	0.945	0.53	0.0405
0.80	1.90	58.7	46.7	233.9	0.199	0.76	12.83	13.59	220.3	0.942	0.51	0.0481
0.99	1.91	59.1	58.3	281.6	0.207	1.17	15.84	17.01	264.6	0.940	0.49	0.0367
0.98	1.90	59.0	57.8	266.4	0.217	0.95	14.30	15.25	251.2	0.943	0.50	0.0456
0.99	1.88	57.6	56.9	250.6	0.227	0.76	13.55	14.32	236.3	0.943	0.52	0.0595
1.31	1.87	57.2	75.1	315.1	0.238	1.17	20.05	21.21	293.9	0.933	0.47	0.0443
1.27	1.86	56.3	71.7	300.2	0.239	0.95	15.84	16.79	283.4	0.944	0.57	0.0519
1.27	1.83	54.6	69.5	284.0	0.245	0.76	15.06	15.82	268.2	0.944	0.59	0.0658
1.49	1.84	55.1	82.1	335.9	0.244	1.17	20.05	21.21	314.7	0.937	0.50	0.0481
1.48	1.81	53.7	79.2	316.6	0.250	0.95	18.31	19.26	297.3	0.939	0.53	0.0620
1.51	1.84	55.4	83.9	348.6	0.241	1.28	20.95	22.23	326.3	0.936	0.49	0.0430
1.64	1.78	52.2	85.5	363.2	0.235	1.28	22.81	24.09	339.1	0.934	0.48	0.0456
1.62	1.78	51.9	84.2	354.9	0.237	1.17	20.05	21.21	333.7	0.940	0.55	0.0481
1.64	1.75	50.5	82.8	333.1	0.248	0.95	18.31	19.26	313.9	0.942	0.59	0.0646

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Table A-9. Compressor Test Data for f = 9 kHz Measurements

Date	f	pa	pa
	kHz	mm-Hg	psi
2/15/91	9	724.6	14.011

V0	i0	fs	2*Vm0	2*im0	T1	T2	Tfm	p1	p2	pfm	Q
volt	amp	kHz	volt	amp	C	C	C	psig	psig	psig	cfm
29	12.03	8.59	40	43	17.3	49.2	12.8	0	16.98	16.77	0.72
27	12.24	8.53	38	40	17.6	48.6	12.3	0	16.68	16.47	0.71
25	12.59	8.4	34	40	17.2	47.2	12	0	16.27	16.06	0.72
23	13.24	8.26	31	40	17.8	45.4	12.1	0	15.74	15.52	0.72
29	13.07	8.55	40	47	16.1	51.4	11.4	0	16.38	16.1	0.93
27	13.46	8.45	38	45	16.2	50.9	11.7	0	16.05	15.78	0.94
25	13.87	8.33	34	42	16.4	49.5	11.5	0	15.56	15.29	0.94
29	14	8.47	40	48	15.6	54.6	11.5	0	15.86	15.52	1.1
27	14.41	8.36	38	46	15.5	53.8	11.5	0	15.47	15.15	1.13
25	14.83	8.26	34	42	15.7	52.3	11.4	0	14.92	14.6	1.11
29	15.07	8.4	40	50	15.6	58.9	11.4	0	15.15	14.77	1.34
27	15.41	8.33	38	48	15.4	58.2	11.5	0	14.69	14.31	1.3

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Table A-10. Compressor Test Data for f = 9 kHz Performance Calculations

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Date	f kHz
2/15/91	9

m g/s	PR	Hs j/g	Ws watt	W0 watt	etas	Wcore watt	Wres watt	Winv watt	Wm watt	etainv	cos (theta)	slip
0.88	2.21	74.3	65.3	348.9	0.187	1.37	18.31	19.68	329.2	0.944	0.51	0.0456
0.86	2.19	73.3	63.1	330.5	0.191	1.15	15.84	16.99	313.5	0.949	0.55	0.0522
0.86	2.16	71.8	61.9	314.8	0.197	0.94	15.84	16.78	298.0	0.947	0.58	0.0667
0.85	2.12	70.2	59.3	304.5	0.195	0.76	15.84	16.60	287.9	0.945	0.62	0.0822
1.12	2.17	71.9	80.3	379.0	0.212	1.37	21.87	23.24	355.8	0.939	0.50	0.0500
1.11	2.15	70.8	79.0	363.4	0.217	1.15	20.05	21.19	342.2	0.942	0.53	0.0611
1.10	2.11	69.2	75.9	346.8	0.219	0.94	17.46	18.41	328.3	0.947	0.61	0.0744
1.29	2.13	70.0	90.6	406.0	0.223	1.37	22.81	24.18	381.8	0.940	0.53	0.0589
1.31	2.10	68.7	90.1	389.1	0.232	1.15	20.95	22.09	367.0	0.943	0.56	0.0711
1.27	2.06	66.8	84.5	370.8	0.228	0.94	17.46	18.41	352.3	0.950	0.66	0.0822
1.54	2.08	67.6	103.9	437.0	0.238	1.37	24.75	26.12	410.9	0.940	0.55	0.0667
1.47	2.05	65.9	96.7	416.1	0.232	1.15	22.81	23.96	392.1	0.942	0.57	0.0744

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Table A-11. Symbols for Measured Quantities

MEASURED QUANTITIES	
f	Electrical Frequency
pa	Ambient Pressure
V0	DC Voltage into Inverter
i0	DC Current into Inverter
fs	Shaft Rotational Frequency
Vm0	Amplitude of Motor Voltage
im0	Amplitude of Motor Current.
T1	Temperature at Compressor Inlet
T2	Temperature at Compressor Exit
Tfm	Temperature at Flowmeter
p1	Pressure at Compressor Inlet
p2	Pressure at Compressor Exit
pfm	Pressure at Flowmeter
Q	Volumetric Flowrate at Flowmeter

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Table A-12. Constants for Performance Calculations

CONSTANTS			
rhostd	Standard Density	1.293	kg/m^3
Tstd	Standard Temperature	273	K
pstd	Standard Pressure	14.696	psi
k	Ratio of Specific Heats	1.402	
cp	Heat Capacity at Constant Press.	1001	j/kg/K
Kres	Inverter Resistive Loss Coeff.	0.00990	
Kcore	Inverter Core Loss Coeff.	0.00181	
ef	Freq. Exponent in Core Loss	1.67	
eb	Field Exponent in Core Loss	2.532	

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Table A-13. Symbols and Equations for Performance Calculations

CALCULATED QUANTITIES		
rhofm	Density at Flowmeter	rhofm = rhostd*(pfm/pstd)/(Tfm/Tstd)
m	Net Mass Flowrate	m = rhofm*Q
PR	Pressure Ratio	PR = p2/p1
Hs	Isentropic Enthalpy Rise	Hs = cp*T1*(PR^((k-1)/k)-1)
Ws	Isentropic Power	Ws = m*Hs
W0	Input Power to Inverter	Wdc = V0*i0
etas	Overall Isentropic Efficiency	etas = Ws/W0
Wcore	Inverter Core Loss	Wcore[watt] = Kcore*V0^eb/fe^(eb-ef) V0[volt], fe[kHz]
Wres	Inverter Resistive Loss	Wres[watt] = Kres*(2*im0)^2 im0[amp]
Winv	Inverter Loss	Winv = Wcore + Wres
Wm	Input Power to Motor	Wm = Wdc-Winv
etainv	Inverter Efficiency	etainv = Wm/Wdc
cos(theta)	Motor Power Factor	cos(theta) = 2/3*Wm/(Vm0*im0)
slip	Motor Slip	slip = (f-fs)/f